

**Programmer guide**

last change on: 2024-03-01

# **CAN - EDCP Programmers guide**

**Description of iseg Enhanced Device Control Protocol to access iseg hardware by CAN bus connection**

## Document history

| Version | Date       | Major changes                                                                                                   |
|---------|------------|-----------------------------------------------------------------------------------------------------------------|
| 2.9     | 2024-03-01 | Added Crate Controller bits for User Input and Output pins. Available from firmware ECH4XA version v4.50        |
| 2.8     | 2023-11-17 | Table 2 Fixed Bit27 to Bit24                                                                                    |
| 2.7     | 2021-03-10 | Fixed PowerMeasure (single/ multiple single read-write access)                                                  |
| 2.6     | 2021-02-17 | Revised flexible groups part<br>Added hardware option bits<br>Added the power nominal, -set, and -measure items |
| 2.5     | 2021-01-12 | Fix "Crate Controller Control" register bit set Crate Enable Active                                             |
| 2.4     | 2020-03-04 | Improve documentation                                                                                           |
| 2.3     | 2020-02-06 | Improve documentation, fixed, Safety Information                                                                |
| 2.2     | 2019-11-08 | Improve documentation, fixed                                                                                    |
| 2.1     | 2017-08-30 | Revised                                                                                                         |
| 2.0     | 2016-01-28 | Relayouted documentation                                                                                        |

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**The information in this manual is subject to change without notice. We take no responsibility for any mistake in the document. We reserve the right to make changes in the product design without reservation and without notification to the users. We decline all responsibility for damages and injuries caused by an improper use of the device.**

# Safety

This section contains important security information for the installation and operation of the device. Failure to follow safety instructions and warnings can result in serious injury or death and property damage.

Safety and operating instructions must be read carefully before starting any operation.

We decline all responsibility for damages and injuries caused which may arise from improper use of our equipment.

## Depiction of the safety instructions

| DANGER!                                                                                          |                                                                                                                                                         |
|--------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
|  <p>DANGER!</p> | <p>"Danger!" indicates a severe injury hazard. The non-observance of safety instructions marked as "Danger!" will lead to possible injury or death.</p> |

| WARNING!                                                                                          |                                                                                                                                                      |
|---------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
|  <p>WARNING!</p> | <p>"Warning!" indicates an injury hazard. The non-observance of safety instructions marked as "Warning!" could lead to possible injury or death.</p> |

| CAUTION!                                                                                            |                                                                                             |
|-----------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------|
|  <p>CAUTION!</p> | <p>Advices marked as "Caution!" describe actions to avoid possible damages to property.</p> |

| INFORMATION                                                                                            |                                                                    |
|--------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------|
|  <p>INFORMATION</p> | <p>Advices marked as "Information" give important information.</p> |



Read the manual.



Attention high voltage!



Important information.

## Intended Use

The device may only be operated within the limits specified in the data sheet. The permissible ambient conditions (temperature, humidity) must be observed. The device is designed exclusively to control high voltage systems as specified in the data sheet. It must only be used specified in Technical data. Any other use not specified by the manufacturer is not intended. The manufacturer is not liable for any damage resulting from improper use.

## Qualification of personnel

A qualified person is someone who is able to assess the work assigned to him, recognize possible dangers and take suitable safety measures on the basis of his technical training, his knowledge and experience as well as his knowledge of the relevant regulations.

## General safety instructions

- Observe the valid regulations for accident prevention and environmental protection.
- Observe the safety regulations of the country in which the product is used.
- Observe the technical data and environmental conditions specified in the product documentation.
- You may only put the product into operation after it has been established that the high-voltage device complies with the country-specific regulations, safety regulations and standards of the application.
- The high-voltage power supply unit may only be installed by qualified personnel.

## Important safety instructions

### DANGER!



DANGER!

This device is part of a high voltage supplying systems.  
High voltages are dangerous and may be fatal.

USE CAUTION WHILE WORKING WITH THIS EQUIPMENT.  
BE AWARE OF ELECTRICAL HAZARDS.

Always follow at the minimum these provisions:

- High voltages must always be grounded
- Do not touch wiring or connectors without securing
- Never remove covers or equipment
- Always observe humidity conditions
- Service must be done by qualified personnel only

### WARNING!



WARNING!

RAMP DOWN VOLTAGES!

Before insertion or removal of crate controller, please make sure, that all voltages are ramped down, modules are switched off and power cord is disconnected.

### CAUTION!



CAUTION!

When controlling, with software, the high voltage systems, make sure that nobody is near the high voltage or can be injured.

### INFORMATION



INFORMATION

Please check the compatibility with the devices used.

# Table of Contents

|                                            |           |
|--------------------------------------------|-----------|
| Document history                           | 2         |
| Disclaimer / Copyright                     | 2         |
| <b>Safety</b>                              | <b>3</b>  |
| Depiction of the safety instructions       | 3         |
| Intended Use                               | 4         |
| Qualification of personnel                 | 4         |
| General safety instructions                | 4         |
| <b>Important safety instructions</b>       | <b>5</b>  |
| <b>1 General information</b>               | <b>11</b> |
| 1.1 Devices covered by this manual         | 11        |
| 1.2 CAN-Bus Implementation                 | 12        |
| <b>2 Crate Controller CC24/23</b>          | <b>13</b> |
| 2.1 Data types                             | 13        |
| 2.2 Access rights                          | 13        |
| 2.3 NMT CAN commands (broadcast messages)  | 13        |
| 2.4 Crate Controller commands              | 14        |
| 2.4.1 Crate Controller Uptime              | 14        |
| 2.4.2 Crate Controller Serial Number       | 14        |
| 2.4.3 Crate Controller Firmware Release    | 14        |
| 2.4.4 Crate Controller Firmware Name       | 14        |
| 2.4.5 Crate Controller Article Description | 15        |
| 2.4.6 Crate Controller Control             | 15        |
| 2.4.7 Crate Controller Status              | 17        |
| 2.4.8 Crate Controller Event Status        | 19        |
| 2.4.9 Crate Controller Event Mask          | 19        |
| 2.4.10 Crate Controller Fan Speed Percent  | 20        |
| 2.4.11 Crate Power On/Off                  | 20        |
| 2.4.12 Crate Chassis Identification        | 20        |
| 2.4.13 Crate Backplane Type                | 21        |
| 2.4.14 Crate Temperature Sensor            | 22        |
| 2.4.15 Crate Supply Measurement            | 22        |
| 2.4.16 Crate Supply Nominal                | 23        |
| 2.5 Statistic registers                    | 24        |
| 2.5.1 CAN Bus Received                     | 24        |
| 2.5.2 CAN Bus Receiver Overrun             | 24        |
| 2.5.3 CAN Bus Transmitted                  | 24        |

|                                                                                                       |           |
|-------------------------------------------------------------------------------------------------------|-----------|
| 2.5.4 CAN Bus Transmit Buffer Full                                                                    | 25        |
| 2.5.5 CAN Bus Dropped                                                                                 | 25        |
| 2.5.6 CAN Bus Error                                                                                   | 25        |
| 2.5.7 CAN Bus Throttle                                                                                | 25        |
| 2.5.8 CAN Bus Status                                                                                  | 26        |
| 2.5.9 CAN Bus Disabled                                                                                | 26        |
| 2.5.10 CAN Bus Bitrate                                                                                | 27        |
| 2.6 Examples                                                                                          | 27        |
| <b>3 Commands for High Voltage Devices</b>                                                            | <b>30</b> |
| 3.1 General information                                                                               | 30        |
| 3.2 General settings and options                                                                      | 30        |
| 3.3 Operation principle                                                                               | 31        |
| 3.3.1 Remote interface control                                                                        | 31        |
| 3.3.2 Channel and Module                                                                              | 32        |
| 3.3.3 Terminology                                                                                     | 32        |
| 3.3.4 Channel operation modes                                                                         | 33        |
| 3.3.5 Status and Event generation                                                                     | 34        |
| 3.3.6 Additional current measuring range (Option)                                                     | 34        |
| 3.3.7 Control and Status items                                                                        | 35        |
| 3.3.7.1 Controls                                                                                      | 35        |
| 3.3.7.2 Status and events                                                                             | 35        |
| 3.3.7.3 Event status and event mask                                                                   | 35        |
| 3.3.8 Summarizing channel characteristics into groups                                                 | 37        |
| 3.3.8.1 Set Group                                                                                     | 37        |
| 3.3.8.2 Status Group                                                                                  | 37        |
| 3.3.8.3 Monitor Group                                                                                 | 37        |
| 3.3.8.4 Timeout Group                                                                                 | 37        |
| 3.3.8.5 Responses on events (Soft-Kill features)                                                      | 37        |
| 3.4 Communication via Interface                                                                       | 38        |
| 3.4.1 Enhanced Device Control Protocol EDCP                                                           | 38        |
| 3.4.1.1 Data formats                                                                                  | 40        |
| 3.4.2 CAN Data Frame                                                                                  | 41        |
| 3.4.3 Summary of CAN data frame accesses via the NMT service identifier                               | 43        |
| 3.4.4 Summary of CAN data frame accesses via the Front-end-address identifier                         | 46        |
| 3.4.4.1 List to access of the EDCP made for HV boards up to 255 channels EDCP Single Channel Accesses | 46        |
| 3.4.4.2 EDCP Multiple Single Channels Access                                                          | 48        |
| 3.4.4.3 Module Access                                                                                 | 50        |
| 3.4.4.4 EDCP Group Accesses                                                                           | 52        |
| 3.4.4.5 Important DCP Module Access                                                                   | 53        |
| 3.5 Description of data information per DATA_ID in EDCP                                               | 54        |
| 3.5.1 EDCP Single Access                                                                              | 54        |
| 3.5.1.1 Channel status (single/multiple single read-write access)                                     | 54        |
| 3.5.1.2 Channel status32 (single/multiple single read-write access)                                   | 54        |

|                                                                                              |    |
|----------------------------------------------------------------------------------------------|----|
| 3.5.1.3 Channel control: (single write- and single/ multiple single read-write access)       | 57 |
| 3.5.1.4 Channel control32: (single write- and single/ multiple single read-write access)     | 57 |
| 3.5.1.5 Channel event status (single write- and single/ multiple single read-write access)   | 58 |
| 3.5.1.6 Channel event status32 (single write- and single/ multiple single read-write access) | 59 |
| 3.5.1.7 Channel event mask (single write- and single/ multiple single read-write access)     | 61 |
| 3.5.1.8 Channel event mask32 (single write- and single/ multiple single read-write access)   | 61 |
| 3.5.1.9 Delayed trip time                                                                    | 63 |
| 3.5.1.10 Delayed trip action (single/ multiple single read-write access)                     | 63 |
| 3.5.1.11 External channel inhibit                                                            | 64 |
| 3.5.1.12 VoltageRampPriority (single write- and single/ multiple single read-write access)   | 64 |
| 3.5.1.13 Set voltage (single write- and single/ multiple single read-write access)           | 65 |
| 3.5.1.14 Set current / trip (single write- and single/ multiple single read-write access)    | 65 |
| 3.5.1.15 Voltage measurement (single/ multiple single read-write access)                     | 66 |
| 3.5.1.16 Current measurement (single/ multiple single read-write access)                     | 66 |
| 3.5.1.17 Voltage bounds (single write- / single/ multiple single read-write access)          | 67 |
| 3.5.1.18 Current bounds (single write- / single/ multiple single read-write access)          | 67 |
| 3.5.1.19 Nominal voltage (single/ multiple single read-write access)                         | 68 |
| 3.5.1.20 Nominal current (single/ multiple single read-write access)                         | 68 |
| 3.5.1.21 Nominal power (single/ multiple single read-write access)                           | 68 |
| 3.5.1.22 Current measurement range (single/ multiple single read-write access)               | 69 |
| 3.5.1.23 VoltageBottom (single/ multiple single read-write access)                           | 69 |
| 3.5.1.24 VCT Coefficient (single/ multiple single read-write access)                         | 70 |
| 3.5.1.25 Temperature external (single/ multiple single read-write access)                    | 70 |
| 3.5.1.26 Resistor external (single/ multiple single read-write access)                       | 71 |
| 3.5.1.27 VoltageRampSpeedUp (single write- / single/ multiple single read-write access)      | 71 |
| 3.5.1.28 VoltageRampSpeedDown (single write- / single/ multiple single read-write access)    | 72 |
| 3.5.1.29 CurrentRampSpeedUp (single write- / single/ multiple single read-write access)      | 72 |
| 3.5.1.30 CurrentRampSpeedDown (single write- / single/ multiple single read-write access)    | 73 |
| 3.5.1.31 VoltageRampSpeedMin (single write- / single/ multiple single read-write access)     | 73 |
| 3.5.1.32 VoltageRampSpeedMax (single write- / single/ multiple single read-write access)     | 74 |
| 3.5.1.33 CurrentRampSpeedMin (single write- / single/ multiple single read-write access)     | 74 |
| 3.5.1.34 CurrentRampSpeedMax (single write- / single/ multiple single read-write access)     | 75 |
| 3.5.1.35 PowerSet (single write- / single/ multiple single read-write access)                | 75 |
| 3.5.1.36 PowerMeasure (single/ multiple single read-write access)                            | 76 |
| 3.5.1.37 Output mode (single/ multiple single read-write access)                             | 76 |
| 3.5.1.38 Output polarity (single/ multiple single read-write access)                         | 77 |
| 3.5.1.39 Output voltage mode (single/ multiple single read-write access)                     | 77 |
| 3.5.1.40 Output current mode (single/ multiple single read-write access)                     | 78 |
| 3.5.1.41 Output voltage mode list (single/ multiple single read-write access)                | 78 |
| 3.5.1.42 Output current mode list (single/ multiple single read-write access)                | 78 |
| 3.5.1.43 Group number (single/ multiple single read-write access)                            | 79 |
| 3.5.2 EDCP Module Accesses                                                                   | 79 |
| 3.5.2.1 ModuleStatus (module read-write access)                                              | 79 |
| 3.5.2.2 ModuleStatus32 (module read-write access)                                            | 80 |
| 3.5.2.3 ModuleControl (module write- / read-write access)                                    | 83 |
| 3.5.2.4 ModuleControl32 (module write- / read-write access)                                  | 83 |

|                                                                                                 |     |
|-------------------------------------------------------------------------------------------------|-----|
| 3.5.2.5 ModuleEventStatus (module write- / read-write access)                                   | 85  |
| 3.5.2.6 ModuleEventStatus32 (single/ multiple single read-write access)                         | 85  |
| 3.5.2.7 ModuleEventMask (module write- / read-write access)                                     | 86  |
| 3.5.2.8 ModuleEventMask32 (module write- / read-write access)                                   | 87  |
| 3.5.2.9 ModuleEventChannelStatus (module write- / read-write access)                            | 88  |
| 3.5.2.10 ModuleEventChannelStatus32 (module write- / read-write access)                         | 88  |
| 3.5.2.11 ModuleEventChannelMask (module write- / read-write access)                             | 89  |
| 3.5.2.12 ModuleEventChannelMask32 (module write- / read-write access)                           | 89  |
| 3.5.2.13 ModuleEventGroupStatus (module write- / read-write access)                             | 90  |
| 3.5.2.14 ModuleEventGroupMask (module write- / read-write access)                               | 91  |
| 3.5.2.15 VoltageRampSpeed (module write- / read-write access)                                   | 92  |
| 3.5.2.16 CurrentRampSpeed – current controlled modules only (module write- / read-write access) | 92  |
| 3.5.2.17 VoltageMax – OPTION (module read-write access)                                         | 93  |
| 3.5.2.18 CurrentMax – OPTION (module read-write access)                                         | 94  |
| 3.5.2.19 Supply24 (module read-write access)                                                    | 94  |
| 3.5.2.20 Supply5 (module read-write access)                                                     | 95  |
| 3.5.2.21 BoardTemperature (module read-write access)                                            | 95  |
| 3.5.2.22 Threshold to arm the errors detection (module write / read- write access)              | 95  |
| 3.5.2.23 Serial number (module read-write access)                                               | 96  |
| 3.5.2.24 Firmware release (module read-write access)                                            | 96  |
| 3.5.2.25 Bit rate (module write- / read-write access)                                           | 96  |
| 3.5.2.26 Firmware Name (module read-write access)                                               | 97  |
| 3.5.2.27 ADC SamplesPerSecond SPS (module write- / read-write access)                           | 98  |
| 3.5.2.28 DigitalFilter (module write- / read-write access)                                      | 98  |
| 3.5.2.29 ChannelNumber (module read access)                                                     | 98  |
| 3.5.2.30 ArticleDescription (module read access)                                                | 99  |
| 3.5.2.31 ModuleOption (module read access)                                                      | 99  |
| 3.5.2.32 ModuleOptionSpec (module read access)                                                  | 101 |
| 3.5.2.33 ModuleCommMode (module write access)                                                   | 102 |
| 3.5.3 EDCP Group Accesses                                                                       | 103 |
| 3.5.3.1 SetGroup                                                                                | 104 |
| 3.5.3.2 StatusGroup                                                                             | 106 |
| 3.5.3.3 MonitoringGroup                                                                         | 108 |
| 3.5.3.4 DelayedTripGroup                                                                        | 111 |
| 3.5.3.5 Request Temperatures and Supplies (group write access)                                  | 113 |
| 3.5.3.6 GroupVoltageLimit – OPTION (module read-write access)                                   | 113 |
| 3.5.3.7 GroupCurrentLimit – OPTION (module read-write access)                                   | 113 |
| 3.5.3.8 VoltageSetAllChannels (group write access)                                              | 114 |
| 3.5.3.9 Current-Trip/Set-AllChannels (group write access)                                       | 114 |
| 3.5.3.10 SetOnOffAllChannels (group write- / read-write access)                                 | 115 |
| 3.5.3.11 SetEmergencyAllChannels (group write- / read-write access)                             | 116 |
| 3.5.3.12 EventStatusVoltageLimitAllChannels (group write- / read-write access)                  | 117 |
| 3.5.3.13 EventStatusCurrentLimitAllChannels (group write- / read-write access)                  | 118 |
| 3.5.3.14 EventStatusCurrentTripAllChannels (group write- / read-write access)                   | 119 |
| 3.5.3.15 EventStatusExternalInhibitAllChannels (group write- / read-write access)               | 120 |
| 3.5.3.16 Set ON / OFF channels extender (group write- / read-write access)                      | 121 |

|                                                                                                                                  |            |
|----------------------------------------------------------------------------------------------------------------------------------|------------|
| 3.5.3.17 Set EMERGENCY channels extender (group write- / read-write access)                                                      | 122        |
| 3.5.4 Important DCP Module Accesses                                                                                              | 123        |
| 3.5.4.1 GeneralStatus (group write- / read-write / active access)                                                                | 123        |
| 3.5.4.2 Log-on / Log-off Front-end device at superior layer (module active- / write access)                                      | 126        |
| 3.5.5 Events                                                                                                                     | 128        |
| 3.5.5.1 Channel events                                                                                                           | 128        |
| 3.5.5.2 Group events (in preparation)                                                                                            | 129        |
| 3.5.5.3 Module events                                                                                                            | 129        |
| <b>4 Appendix</b>                                                                                                                | <b>131</b> |
| 4.1 A – Shortcuts                                                                                                                | 131        |
| 4.2 Appendix B – Diagram of operating modes                                                                                      | 132        |
| 4.3 Appendix C – Programming flowchart to store the settings permanently with help of General state save bit                     | 133        |
| 4.4 Appendix D – Programming flowchart to store the configurations of the module permanently with help of General state save bit | 134        |
| 4.5 Appendix E – Literature references                                                                                           | 135        |
| <b>5 Manufacturer contact</b>                                                                                                    | <b>135</b> |

# 1 General information

This Manual describes for one the CAN - EDCP crate controller commands and for the other the CAN - EDCP commands for High Voltage Devices.

## 1.1 Devices covered by this manual

All devices described in this manual have in common, that they support the CAN - EDCP (Enhanced device communication protocol for Controller Area Network).

- CC24 is the crate controller card for the 19" master crates with the iCS-2 (iseq Communication Server 2)
- CC23 is the crate controller card for the 19" slave crates
- EHS combines standard or high precision, high voltage sources in 19" format with fix or mixed output polarity, up to 32 channels per module are possible
- EHS FLEX combines standard or high precision, high voltage sources in 19" format with fix or mixed output polarity, up to 48 channels per module are possible
- EHS STACK combines standard or high precision, high voltage sources in 19" format with fix or mixed output polarity, up to 16 channels per module are possible
- EBS combines standard, bipolar current sink and high voltage sources in 19" format, up to 24 channels per module are possible
- EDS combines standard high voltage sources with fix output polarity, up to 48 channels per module are possible
- NHS combines standard or high precision high voltage sources in NIM format with fix or mixed output polarity, up to 6 channels per module are possible
- NHR combines standard or high precision high voltage sources in NIM format with switchable output polarity, up to 4 channels per module are possible

## 1.2 CAN-Bus Implementation

The data frame structure is matched to the message frame of the standard-format according to CAN specification 2.0B.

The data frame of the EDCP will be transferred as data word with n bytes length in the data field of the CAN frame according to the specific demand of the related access. Therefore this results into a Data Length Code (DLC) of the CAN-protocol of n.

The 11 bit identifier of the CAN protocol will be used for addressing of the Front-end devices and classification of data write, data request, data reply and alarm messages.

In following every bit of the 11 bit identifier will be described:

|          |   |                             |
|----------|---|-----------------------------|
| ID10 (C) | 1 | Crate controller command    |
|          | 0 | High voltage source command |
| ID9 (P)  | 1 | Alarm                       |
|          | 0 | Normal messages             |

Notes:

ID8 to ID3 (A5..A0) allow the addressing of 64 Front-end devices (ID3: Address bit 0;...; ID8: Address bit 5)

|                |   |                                                                      |
|----------------|---|----------------------------------------------------------------------|
| ID2 (NMT)      | 1 | Send a broadcast message defined as network management message (NMT) |
|                | 0 | Normal or alarm message                                              |
| ID1            | 1 | Reply of a data request                                              |
|                | 0 | No data request                                                      |
| ID0 (DATA_DIR) | 1 | Data request                                                         |
|                | 0 | Data write                                                           |

That means all "even" CAN-ports (Identifier) are interpreted as 'Write ports' all "odd" CAN ports as 'Read ports'.

Only if the Front-end device is not registered at the controller or if it does not receive valid data during a longer time period (ca. 1 min), then it will actively send the registration frame with DATA\_DIR = 1. The RTR Bit is always set to zero.

In one CAN segment modules with unequal identifier and equal bit rate are allowed only. The factory fixed bit rate is written on the sticker at the side panel.

## 2 Crate Controller CC24/23

### 2.1 Data types

|       |                                                     |
|-------|-----------------------------------------------------|
| UI1:  | One byte unsigned integer (8 bit)                   |
| CHAR: | One ASCII character (8 bit)                         |
| UI4:  | Four byte unsigned integer (32 bit)                 |
| R4:   | Four byte floating point IEEE-754, single precision |

All data on the CAN bus is in big endian format, i.e. for UI4 and R4, the highest data byte is transmitted first.

### 2.2 Access rights

|       |                                                  |
|-------|--------------------------------------------------|
| R =   | Read only: the register can only be read         |
| R/W = | Read/write: the register can be read and written |
| R/C = | Read/clear: the register can be read and cleared |

### 2.3 NMT CAN commands (broadcast messages)

The following NMT commands (CAN-ID 0x004) are handled by the Crate Controller:

- NMT\_DATAID\_START (0xC4)
  - Switches from stop mode to normal operation
  - Message is forwarded to the backplane (and therefore to the modules)
- NMT\_DATAID\_STOP (0xC8)
  - Switches from normal operation to stop mode to allow the command NMT\_RESET\_CAN
  - Message is forwarded to the backplane (and therefore to the modules)
- NMT\_DATAID\_RESET\_CAN (0xCC)
  - Re-initializes all CAN interfaces
  - Clears all transmit buffer
  - Clears all statistic registers
  - Message is forwarded to the backplane (and therefore to the modules)
  - Re-initializes the modules CAN interface
  - Modules starts to send their Log-On message

A short delay (10 milliseconds) should be kept between the commands NMT\_STOP and NMT\_RESET\_CAN, so that all messages can be forwarded correctly to the modules.

## 2.4 Crate Controller commands

### 2.4.1 Crate Controller Uptime

Crate Controller Uptime 0x1113 UI4 R

This register returns the crate controllers uptime in seconds.

| Access  | CAN-ID | DLC | DATA_ID | Data_3           | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|------------------|--------|--------|--------|
| Request | 0x601  | 2   | 0x1113  |                  |        |        |        |
| Answer  | 0x604  | 6   | 0x1113  | Crate Uptime UI4 |        |        |        |

Table 1

### 2.4.2 Crate Controller Serial Number

Crate Controller Serial Number 0x1200 UI4 R

This register returns the crate controllers serial number.

| Access  | CAN-ID | DLC | DATA_ID | Data_3                  | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|-------------------------|--------|--------|--------|
| Request | 0x601  | 2   | 0x1200  |                         |        |        |        |
| Answer  | 0x604  | 6   | 0x1200  | Crate Serial Number UI4 |        |        |        |

Table 2

### 2.4.3 Crate Controller Firmware Release

Crate Controller Firmware Release 0x1201 UI1[4] R

This register returns the crate controllers firmware release.

| Access  | CAN-ID | DLC | DATA_ID | Data_3    | Data_2    | Data_1    | Data_0    |
|---------|--------|-----|---------|-----------|-----------|-----------|-----------|
| Request | 0x601  | 2   | 0x1201  |           |           |           |           |
| Answer  | 0x604  | 6   | 0x1201  | Release 1 | Release 2 | Release 3 | Release 4 |

Table 3

### 2.4.4 Crate Controller Firmware Name

Crate Controller Firmware Name 0x1203 CHAR[6] R

This register returns the crate controllers firmware name.

| Access  | CAN-ID | DLC | DATA_ID | Data_5 | Data_4 | Data_3 | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|--------|--------|--------|--------|--------|--------|
| Request | 0x601  | 2   | 0x1203  |        |        |        |        |        |        |
| Answer  | 0x604  | 8   | 0x1203  | 'E'    | 'C'    | 'H'    | '4'    | 'x'    | 'A'    |

Table 4

## 2.4.5 Crate Controller Article Description

Crate Controller Article Description

0x1209

CHAR[]

R

This register returns the crate controllers article description. Depending on the length of the article description, multiple CAN messages may be sent. The description is terminated by a zero character.

| Access  | CAN-ID | DLC   | DATA_ID | Data_5 | Data_4 | Data_3 | Data_2 | Data_1 | Data_0 |
|---------|--------|-------|---------|--------|--------|--------|--------|--------|--------|
| Request | 0x601  | 2     | 0x1209  |        |        |        |        |        |        |
| Answer  | 0x604  | 3...8 | 0x1209  | 0      | 'C'    | 'C'    | '2'    | '4'    | 0      |

Table 5

## 2.4.6 Crate Controller Control

Crate Controller Control

0x1A01

UI4

R/W

The register Crate Controller Control sets crate functions.

| Access  | CAN-ID | DLC | DATA_ID | Data_3            | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|-------------------|--------|--------|--------|
| Request | 0x601  | 2   | 0x1A01  |                   |        |        |        |
| Answer  | 0x604  | 6   | 0x1A01  | Crate Control UI4 |        |        |        |
| Set     | 0x600  | 6   | 0x1A01  | Crate Control UI4 |        |        |        |

Table 6

| Bit31   | Bit30   | Bit29              | Bit28           | Bit27                | Bit26             | Bit25                      | Bit24                   |
|---------|---------|--------------------|-----------------|----------------------|-------------------|----------------------------|-------------------------|
| res (0) | res (0) | do Set Legacy Mode | set Legacy Mode | do Set Auto Power On | set Auto Power On | do Set Crate Enable Active | set Crate Enable Active |
| Bit23   | Bit22   | Bit21              | Bit20           | Bit19                | Bit18             | Bit17                      | Bit16                   |
| res (0) | res (0) | res (0)            | res (0)         | res (0)              | res (0)           | res (0)                    | res (0)                 |
| Bit15   | Bit14   | Bit13              | Bit12           | Bit11                | Bit10             | Bit09                      | Bit08                   |
| res (0) | res (0) | res (0)            | res (0)         | do Set User Output 1 | set User Output 1 | do Set User Output 0       | set User Output 0       |
| Bit07   | Bit06   | Bit05              | Bit04           | Bit03                | Bit02             | Bit01                      | Bit00                   |
| res (0) | res (0) | res (0)            | res (0)         | res (0)              | res (0)           | do Clear Statistic         | do Clear Events         |

Table 7: Crate Controller Control register

| Control Bit                | Description                                                                                                                                                                                                                                                                                                                                                                                 |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| do Clear Events            | Clears the crates event status register. This bit can only be written, it always reads zero.                                                                                                                                                                                                                                                                                                |
| do Clear Statistic         | Clears the crates statistic registers. This bit can only be written, it always reads zero.                                                                                                                                                                                                                                                                                                  |
| set Crate Enable Active    | If this bit is set to one, the high voltage channels can only be turned on, if the pin Crate Enable at the CONTROL connector is pulled high. This bit can only be changed if the backplane is powered off and the bit do Set Crate Enable Active is set to one.                                                                                                                             |
| do Set Crate Enable Active | This bit masks the bit set Crate Enable Active. If this bit is zero, the bit set Crate Enable Active is ignored. This bit can only be written, it always reads zero.                                                                                                                                                                                                                        |
| set Auto Power On          | If this bit is set to one, the backplane is automatically turned on after the mains line is plugged in. Otherwise, the backplane stays off and must be turned on by the POWER ON switch or by remote control. This bit can only be changed if the bit do Set Auto Power On is set to one.                                                                                                   |
| do Set Auto Power On       | This bit masks the bit set Auto Power On. If this bit is zero, the bit set Auto Power On is ignored. This bit can only be written, it always reads zero.                                                                                                                                                                                                                                    |
| set Legacy Mode            | If this bit is set to one, the controller operates in Legacy Mode. In this mode, the modules can be controlled by CAN bus connected to CAN1 or CAN2. Note that in this mode, the internal services like isegHAL, iCSservice, SNMP, EPICS can not be used to control the modules. This bit can only be changed if the backplane is powered off and the bit do Set Legacy Mode is set to one. |
| do Set Legacy Mode         | This bit masks the bit set Legacy Mode. If this bit is zero, the bit set Legacy Mode is ignored. This bit can only be written, it always reads zero.                                                                                                                                                                                                                                        |
| set User Output 0          | The user output pin 0 is set to this value.                                                                                                                                                                                                                                                                                                                                                 |
| do Set User Output 0       | This bit masks the bit set User Output 0. If this bit is zero, the bit set User Output 0 is ignored. This bit can only be written, it always reads zero.                                                                                                                                                                                                                                    |
| set User Output 1          | The user output pin 1 is set to this value.                                                                                                                                                                                                                                                                                                                                                 |
| do Set User Output 1       | This bit masks the bit set User Output 1. If this bit is zero, the bit set User Output 1 is ignored. This bit can only be written, it always reads zero.                                                                                                                                                                                                                                    |

Table 8: Crate Controller Control bit descriptions

## 2.4.7 Crate Controller Status

Crate Controller Status

0x1A00

UI4

R

The Crate Controller Status contains the *actual* status. The bits will be set or reset depending on the crates status.

| Access  | CAN-ID | DLC | DATA_ID | Data_3           | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|------------------|--------|--------|--------|
| Request | 0x601  | 2   | 0x1A00  |                  |        |        |        |
| Answer  | 0x604  | 6   | 0x1A00  | Crate Status UI4 |        |        |        |

Table 9

| Bit31            | Bit30         | Bit29              | Bit28             | Bit27              | Bit26              | Bit25                   | Bit24                |
|------------------|---------------|--------------------|-------------------|--------------------|--------------------|-------------------------|----------------------|
| User Output 1    | User Output 0 | User Input 1       | User Input 0      | CAN Bus Error CAN2 | CAN Bus Error CAN1 | CAN Bus Error Backplane | CAN Bus Error Apalis |
| Bit23            | Bit22         | Bit21              | Bit20             | Bit19              | Bit18              | Bit17                   | Bit16                |
| res (0)          | res (0)       | Crate Fast Off     | Crate Enabled     | Shut Down          | High Voltage On    | Power Fail              | Power On             |
| Bit15            | Bit14         | Bit13              | Bit12             | Bit11              | Bit10              | Bit09                   | Bit08                |
| res (0)          | res (0)       | res (0)            | Sum Error         | High +3.3 CC       | Low +3.3 CC        | High +5 CC              | Low +5 CC            |
| Bit07            | Bit06         | Bit05              | Bit04             | Bit03              | Bit02              | Bit01                   | Bit00                |
| High Temperature | Service       | High +24 Backplane | Low +24 Backplane | High +5 Backplane  | Low +5 Backplane   | High +24 Battery        | Low +24 Battery      |

Table 10: Crate Controller Status

| Status Bit              | Description                                                                                                                                                                                                                                      |
|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CAN Bus Error Apalis    | The internal CAN bus between the Crate Controller and the Apalis is in error state                                                                                                                                                               |
| CAN Bus Error Backplane | The internal CAN bus between the Crate Controller and the HV modules is in error state                                                                                                                                                           |
| CAN Bus Error CAN1      | The external CAN bus connected to CAN1 is in error state                                                                                                                                                                                         |
| CAN Bus Error CAN2      | The external CAN bus connected to CAN2 is in error state                                                                                                                                                                                         |
| High-Voltage-On         | Backplane is powered on and at least one channel within the crate has Status.isOn or measured voltage > 63 V The front panel LED HV-ON is derived from this bit.                                                                                 |
| Power-On                | Backplane is powered on (modules are supplied with voltage)<br>The front panel LED Status lights green when Power-On is set and no supply error exists.<br>The front panel LED Status lights red when Power-On is set and a supply error exists. |
| Power-Fail              | AC line power fail detected.<br>Crate without UPS: high voltage is turned fast off<br>Crate with UPS: high voltage is turned off with ramp after the wait time                                                                                   |
| High Temperature        | At least one modules or the crate controller have high temperature. The high voltage is turned off with the configured voltage ramp speed.                                                                                                       |
| Shut Down               | If the front button POWER ON is pressed for more than 10 seconds, this bit is set for approx. 1 minute. This is used to perform a shut down of the embedded crate computer.                                                                      |
| Sum Error               | This bit is set, whenever one of the bits Power Fail, High Temperature, Service, High Supply, Low Supply or Crate Fast Off is set or if Crate Enabled is cleared.                                                                                |
| Service                 | A fatal error occurred. Contact service.                                                                                                                                                                                                         |

|                |                                                                                                                                                                                                                         |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| High Supply X  | Measured voltage X exceeds the upper limit.                                                                                                                                                                             |
| Low Supply X   | Measured voltage X exceeds the lower limit.                                                                                                                                                                             |
| Crate Enabled  | If the crate is enabled, it is possible to turn on high voltage for all channels. The crate is enabled, if the Crate Control bit set Crate Enable Active is not set, or if the CONTROL pin Crate Enable is pulled high. |
| Crate Fast Off | If the CONTROL pin Crate Fast Off is turned high, the high voltages are shut down without ramp.                                                                                                                         |
| User Input 0   | The user input pin 0 state <sup>1</sup>                                                                                                                                                                                 |
| User Input 1   | The user input pin 1 state                                                                                                                                                                                              |
| User Output 0  | The user output pin 0 state                                                                                                                                                                                             |
| User Output 1  | The user output pin 1 state                                                                                                                                                                                             |

Table 11: Crate Controller Status Bit description

<sup>1</sup> Supported from firmware ECH4XA version v4.50

## 2.4.8 Crate Controller Event Status

Crate Controller Event Status

0x1A02

UI4

R/C

The Event Status bits are set together with the status bits. Unlike Status bits, Event Status bits are not reset automatically. They have to be reset by the user, by writing an 1 to this event bit. All Event Status bits are reset by the Crate Control bit do Clear. The Bits for User Input and Output (28 - 31) are always set when the status of the respective status bit changes.

| Access  | CAN-ID | DLC | DATA_ID | Data_3                 | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|------------------------|--------|--------|--------|
| Request | 0x601  | 2   | 0x1A02  |                        |        |        |        |
| Answer  | 0x604  | 6   | 0x1A02  | Crate Event Status UI4 |        |        |        |
| Clear   | 0x600  | 6   | 0x1A02  | Crate Event Status UI4 |        |        |        |

Table 12

| Bit31            | Bit30         | Bit29              | Bit28             | Bit27             | Bit26            | Bit25            | Bit24           |
|------------------|---------------|--------------------|-------------------|-------------------|------------------|------------------|-----------------|
| User Output 1    | User Output 0 | User Input 1       | User Input 0      | res (0)           | res (0)          | res (0)          | res (0)         |
| Bit23            | Bit22         | Bit21              | Bit20             | Bit19             | Bit18            | Bit17            | Bit16           |
| res (0)          | res (0)       | res (0)            | res (0)           | Shut Down         | High Voltage On  | Power Fail       | Power On        |
| Bit15            | Bit14         | Bit13              | Bit12             | Bit11             | Bit10            | Bit09            | Bit08           |
| res (0)          | res (0)       | res (0)            | Sum Error         | High +3.3 CC      | Low +3.3 CC      | High +5 CC       | Low +5 CC       |
| Bit07            | Bit06         | Bit05              | Bit04             | Bit03             | Bit02            | Bit01            | Bit00           |
| High Temperature | Service       | High +24 Backplane | Low +24 Backplane | High +5 Backplane | Low +5 Backplane | High +24 Battery | Low +24 Battery |

Table 13

## 2.4.9 Crate Controller Event Mask

Crate Controller Event Mask

0x1A3

UI4

R/W

The Event Mask is defined for compatibility to the module EDCP command set, but not used at the moment.

| Access  | CAN-ID | DLC | DATA_ID | Data_3               | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|----------------------|--------|--------|--------|
| Request | 0x601  | 2   | 0x1A03  |                      |        |        |        |
| Answer  | 0x604  | 6   | 0x1A03  | Crate Event Mask UI4 |        |        |        |
| Set     | 0x600  | 6   | 0x1A03  | Crate Event Mask UI4 |        |        |        |

Table 14

## 2.4.10 Crate Controller Fan Speed Percent

Crate Controller Fan Speed Percent

0x1A04

R4

R

This register returns the crates fan speed in percent (0...100). The fan speed is regulated according to the maximum crate temperature. The maximum temperature is collected over all modules and the crate controller. The maximum fan speed is reached at approx. 45° C.

| Access  | CAN-ID | DLC | DATA_ID | Data_3             | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|--------------------|--------|--------|--------|
| Request | 0x601  | 2   | 0x1A04  |                    |        |        |        |
| Answer  | 0x604  | 6   | 0x1A04  | Crate Fan Speed R4 |        |        |        |

Table 15

## 2.4.11 Crate Power On/Off

Crate Power On/Off

0x1A05

UI1

R/W

This register controls the crates power on (1) or off (0) function.

| Access  | CAN-ID | DLC | Data_ID | Data_0 |
|---------|--------|-----|---------|--------|
| Request | 0x601  | 2   | 0x1A05  |        |
| Answer  | 0x604  | 3   | 0x1A05  | 0x00   |
|         |        |     |         |        |
| Set On  | 0x600  | 3   | 0x1A05  | 0x01   |
| Set Off | 0x600  | 3   | 0x1A05  | 0x00   |

Table 16

## 2.4.12 Crate Chassis Identification

Crate Controller Chassis Identification

0x1A06

UI6

R

This register contains the 1-Wire serial number that is read from the crate chassis. This number is an unique number for every crate. The six bytes are the 1-Wire serial number without manufacturer code and without CRC.

This register is filled once the backplane was turned on for at least ten seconds.

| Access  | CAN-ID | DLC | DATA_ID | Data_5                           | Data_4 | Data_3 | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|----------------------------------|--------|--------|--------|--------|--------|
| Request | 0x601  | 2   | 0x1A06  |                                  |        |        |        |        |        |
| Answer  | 0x604  | 8   | 0x1A06  | Crate Chassis Identification UI6 |        |        |        |        |        |

Table 17

## 2.4.13 Crate Backplane Type

Crate Backplane Type

0x1A07

UI2

R/C

This register contains the backplane type for the master and all slave crates.

| Access  | CAN-ID | DLC | DATA_ID | Data_1                   | Data_0 |
|---------|--------|-----|---------|--------------------------|--------|
| Request | 0x601  | 2   | 0x1A07  |                          |        |
| Answer  | 0x604  | 4   | 0x1A07  | Crate Backplane Type UI2 |        |
| Clear   | 0x600  | 2   | 0x1A07  |                          |        |

Table 18

A write access to this register forces a new scan of the backplane type register. It takes approx. two seconds to scan the system and fill the register again.

| Bit31    | Bit30    | Bit29          | Bit28          | Bit27          | Bit26          | Bit25          | Bit24         |
|----------|----------|----------------|----------------|----------------|----------------|----------------|---------------|
|          |          |                |                |                |                |                |               |
| Bit23    | Bit22    | Bit21          | Bit20          | Bit19          | Bit18          | Bit17          | Bit16         |
|          |          |                |                |                |                |                |               |
| Bit15    | Bit14    | Bit13          | Bit12          | Bit11          | Bit10          | Bit09          | Bit08         |
| Reserved | Reserved | Reserved       | Green Slave 5  | Green Slave 4  | Green Slave 3  | Green Slave 2  | Green Slave 1 |
| Bit07    | Bit06    | Bit05          | Bit04          | Bit03          | Bit02          | Bit01          | Bit00         |
| Reserved | Reserved | Yellow Slave 5 | Yellow Slave 4 | Yellow Slave 3 | Yellow Slave 2 | Yellow Slave 1 | Master        |

Table 19

| Bit meaning  |                                 |                                   |
|--------------|---------------------------------|-----------------------------------|
| 0            | Backplane type iseg:            | backplane is sequential           |
| 1            | Backplane type wiener:          | backplane is not sequential       |
| Bit position |                                 |                                   |
| 0            | Master crate                    |                                   |
| 1...5        | Slave crates on CAN line yellow | = (1 = Slave 0, 2 = Slave 1, ...) |
| 8...12       | Slave crates on CAN line green  | = (8 = Slave 0, 9 = Slave 1, ...) |

Table 20

## 2.4.14 Crate Temperature Sensor

Crate Temperature Sensor

0x2001

R4

R

This register contains the actual temperature for different sensors.

Sensor 0 and 1 are placed at the crate controller. Sensor 2 is the maximum temperature in the crate (collected over all modules and the crate controller). The maximum temperature is used to control the crates fan speeds.

If the request is done with DLC = 2, all temperature sensors are returned in three CAN messages. If the request is done with DLC = 3 and a specific sensor, only this sensor is returned.

| Access  | CAN-ID | DLC | DATA_ID | Sensor | Data_3                 | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|--------|------------------------|--------|--------|--------|
| Request | 0x601  | 2   | 0x2001  |        |                        |        |        |        |
| Answer  | 0x604  | 7   | 0x2001  | 0x00   | Crate Temperature 0 R4 |        |        |        |
|         | 0x604  | 7   | 0x2001  | 0x01   | Crate Temperature 1 R4 |        |        |        |
|         | 0x604  | 7   | 0x2001  | 0x02   | Crate Temperature 2 R4 |        |        |        |
|         |        |     |         |        |                        |        |        |        |
| Request | 0x601  | 3   | 0x2001  | 0x01   |                        |        |        |        |
| Answer  | 0x604  | 7   | 0x2001  | 0x01   | Crate Temperature 0 R4 |        |        |        |

Table 21

## 2.4.15 Crate Supply Measurement

Crate Supply Measurement

0x2002

R4

R

This register contains the measured supply voltages.

If the request is done with DLC = 2, all supply measurement values are returned in consecutive CAN messages. If the request is done with DLC = 3 and a specific supply number, only this measurement value is returned.

| Access  | CAN-ID | DLC | DATA_ID | Supply | Data_3                        | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|--------|-------------------------------|--------|--------|--------|
| Request | 0x601  | 2   | 0x2002  |        |                               |        |        |        |
| Answer  | 0x604  | 7   | 0x2002  | 0x00   | Crate Supply Measurement 0 R4 |        |        |        |
|         | 0x604  | 7   | 0x2002  | 0x01   | ...                           |        |        |        |
|         | 0x604  | 7   | 0x2002  | 0x08   | Crate Supply Measurement 8 R4 |        |        |        |

Table 22

## 2.4.16 Crate Supply Nominal

Crate Supply Nominal

0x2003

R4

R

This register contains the nominal supply voltages.

If the request is done with DLC = 2, all supply nominal values are returned in consecutive CAN messages. If the request is done with DLC = 3 and a specific supply number, only this nominal value is returned.

| Access  | CAN-ID | DLC | DATA_ID | Supply | Data_3                    | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|--------|---------------------------|--------|--------|--------|
| Request | 0x601  | 2   | 0x2003  |        |                           |        |        |        |
| Answer  | 0x604  | 7   | 0x2003  | 0x00   | Crate Supply Nominal 0 R4 |        |        |        |
|         | 0x604  | 7   | 0x2003  | 0x01   | ...                       |        |        |        |
|         | 0x604  | 7   | 0x2003  | 0x08   | Crate Supply Nominal 8 R4 |        |        |        |

Table 23

## 2.5 Statistic registers

For each CAN bus, multiple statistic registers are kept. The Crate Controller owns four CAN busses, which are numbered the following way:

- 0) CAN PC
- 1) CAN Backplane
- 2) CAN 2
- 3) CAN 1

The existing statistic registers are described below.

If a request message without a CAN bus number (DLC = 2) is received, the statistic register for all four CAN busses are returned.

The statistic counter are incremented by the crate controller and can be reset by the NMT command NMT\_CAN\_RESET together with the CAN interfaces or by the Crate Control bit do Clear Statistic.

### 2.5.1 CAN Bus Received

CAN Bus Received 0x2040 UI4 R

This register counts the received messages for the given CAN bus.

| Access  | CAN-ID | DLC | DATA_ID | CAN bus | Data_3                | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|---------|-----------------------|--------|--------|--------|
| Request | 0x601  | 3   | 0x2040  | 00      |                       |        |        |        |
| Answer  | 0x604  | 7   | 0x2040  | 00      | Received Messages UI4 |        |        |        |

Table 24

### 2.5.2 CAN Bus Receiver Overrun

CAN Bus Receiver Overrun 0x2041 UI4 R

This register counts the receive buffer overruns for the given CAN bus. A receive buffer overrun occurs, if a CAN message could not be read in time from the CAN bus.

This register should always be zero.

| Access  | CAN-ID | DLC | DATA_ID | CAN bus | Data_3                        | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|---------|-------------------------------|--------|--------|--------|
| Request | 0x601  | 3   | 0x2041  | 00      |                               |        |        |        |
| Answer  | 0x604  | 7   | 0x2041  | 00      | Receiver Overrun Messages UI4 |        |        |        |

Table 25

### 2.5.3 CAN Bus Transmitted

CAN Bus Transmitted 0x2042 UI4 R

This register counts the transmitted messages for the given CAN bus.

| Access  | CAN-ID | DLC | DATA_ID | CAN bus | Data_3                   | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|---------|--------------------------|--------|--------|--------|
| Request | 0x601  | 3   | 0x2042  | 00      |                          |        |        |        |
| Answer  | 0x604  | 7   | 0x2042  | 00      | Transmitted Messages UI4 |        |        |        |

Table 26

## 2.5.4 CAN Bus Transmit Buffer Full

CAN Bus Transmit Buffer Full 0x2043 UI4 R

This register counts the messages, that could not be sent to the given CAN bus because of full transmit buffer.

| Access  | CAN-ID | DLC | DATA_ID | CAN bus | Data_3                   | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|---------|--------------------------|--------|--------|--------|
| Request | 0x601  | 3   | 0x2043  | 00      |                          |        |        |        |
| Answer  | 0x604  | 7   | 0x2043  | 00      | Transmit Buffer Full UI4 |        |        |        |

Table 27

## 2.5.5 CAN Bus Dropped

CAN Bus Dropped 0x2044 UI4 R

This register counts the messages that were received from the given CAN bus and could not be routed because of unclear destination.

This register should always be zero.

| Access  | CAN-ID | DLC | DATA_ID | CAN bus | Data_3               | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|---------|----------------------|--------|--------|--------|
| Request | 0x601  | 3   | 0x2044  | 00      |                      |        |        |        |
| Answer  | 0x604  | 7   | 0x2044  | 00      | Dropped Messages UI4 |        |        |        |

Table 28

## 2.5.6 CAN Bus Error

CAN Bus Error 0x2045 UI4 R

This register is incremented every second when the given CAN bus is in error state.

| Access  | CAN-ID | DLC | DATA_ID | CAN bus | Data_3            | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|---------|-------------------|--------|--------|--------|
| Request | 0x601  | 3   | 0x2045  | 00      |                   |        |        |        |
| Answer  | 0x604  | 7   | 0x2045  | 00      | Error Seconds UI4 |        |        |        |

Table 29

## 2.5.7 CAN Bus Throttle

CAN Bus Throttle 0x2046 UI4 R

This register counts the number of generated throttle messages for the given CAN bus.

| Access  | CAN-ID | DLC | DATA_ID | CAN bus | Data_3                | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|---------|-----------------------|--------|--------|--------|
| Request | 0x601  | 3   | 0x2046  | 00      |                       |        |        |        |
| Answer  | 0x604  | 7   | 0x2046  | 00      | Throttle Messages UI4 |        |        |        |

Table 30

## 2.5.8 CAN Bus Status

CAN Bus Status

0x2047

UI4

R

This register holds the current status for the given CAN bus.

| Access  | CAN-ID | DLC | DATA_ID | CAN bus | Data_3         | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|---------|----------------|--------|--------|--------|
| Request | 0x601  | 3   | 0x2047  | 00      | 1              | 2      | 3      | 4      |
| Answer  | 0x604  | 7   | 0x2047  | 00      | Bus Status UI4 |        |        |        |

Table 31

The CAN Bus Status register contains the following information:

- Receiver bus status: Ok (0), Warning (1), Error (2), Bus off (3)
- Transmitter bus status: Ok (0), Warning (1), Error (2), Bus off (3)
- CAN hardware activated
- CAN hardware synchronized with CAN bus
- CAN hardware in special mode (initializing, sleep, listen-only, loopback).  
These bits should not be set in normal operation conditions.

The CAN hardware status is refreshed at the time of the request.

| Bit31                                                                | Bit30 | Bit29    | Bit28       | Bit27   | Bit26        | Bit25    | Bit24        |
|----------------------------------------------------------------------|-------|----------|-------------|---------|--------------|----------|--------------|
|                                                                      |       |          |             |         |              |          |              |
| Bit23                                                                | Bit22 | Bit21    | Bit20       | Bit19   | Bit18        | Bit17    | Bit16        |
|                                                                      |       | Loopback | Listen Only | Enabled | Synchronized | Sleeping | Initializing |
| Bit15                                                                | Bit14 | Bit13    | Bit12       | Bit11   | Bit10        | Bit09    | Bit08        |
| Transmitter bus status (0 = Ok, 1 = Warning, 2 = Error, 3 = Bus off) |       |          |             |         |              |          |              |
| Bit07                                                                | Bit06 | Bit05    | Bit04       | Bit03   | Bit02        | Bit01    | Bit00        |
| Receiver bus status (0 = Ok, 1 = Warning, 2 = Error, 3 = Bus off)    |       |          |             |         |              |          |              |

Table 32

## 2.5.9 CAN Bus Disabled

CAN Bus Disabled

0x2048

UI4

R

This register counts the number of dropped messages because the given CAN bus is not enabled (e.g. backplane is off).

| Access  | CAN-ID | DLC | DATA_ID | CAN bus | Data_3                | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|---------|-----------------------|--------|--------|--------|
| Request | 0x601  | 3   | 0x2048  | 00      |                       |        |        |        |
| Answer  | 0x604  | 7   | 0x2048  | 00      | Disabled Messages UI4 |        |        |        |

Table 33

## 2.5.10 CAN Bus Bitrate

CAN Bus Bitrate 0x2049 UI4 R

This register holds the current bit rate for the given CAN bus.

| Access  | CAN-ID | DLC | DATA_ID | CAN bus | Data_3      | Data_2 | Data_1 | Data_0 |
|---------|--------|-----|---------|---------|-------------|--------|--------|--------|
| Request | 0x601  | 3   | 0x2049  | 00      |             |        |        |        |
| Answer  | 0x604  | 7   | 0x2049  | 00      | Bitrate UI4 |        |        |        |

Table 34

## 2.6 Examples

CC = Crate-Controller, PC = Controlling PC

| Message             | Direction | CAN-ID | DLC | Data ID | Data | Data | Data | Data |
|---------------------|-----------|--------|-----|---------|------|------|------|------|
| Log-On Request      | CC → PC   | 601    | 3   | D8 00   | 2E   |      |      |      |
| Log-On Confirmation | CC → PC   | 600    | 2   | D8 01   |      |      |      |      |
| Status Request      | PC → CC   | 601    | 2   | 1A 00   |      |      |      |      |
| Status Answer       | CC → PC   | 604    | 6   | 1A 00   | 00   | 00   | 00   | 00   |
| Crate Power On      | PC → CC   | 600    | 3   | 1A 05   | 01   |      |      |      |
| Crate Power Off     | PC → CC   | 600    | 3   | 1A 05   | 00   |      |      |      |
| Fan Speed Request   | PC → CC   | 601    | 2   | 1A 04   |      |      |      |      |
| Fan Speed Answer    | CC → PC   | 604    | 6   | 1A 04   | 40   | A0   | 00   | 00   |

Table 35: Examples

## Request Temperatures and Supplies (group request)

| Message                       | CAN-ID | DLC | DataID | Channel | Data | Data | Data | Data | Value   |
|-------------------------------|--------|-----|--------|---------|------|------|------|------|---------|
| Request all Temperatures      | 601    | 2   | 20 01  |         |      |      |      |      |         |
| Temperature 0                 | 604    | 7   | 20 01  | 00      | 41   | EF   | 0D   | B0   | 29.9 °C |
| Temperature 1                 | 604    | 7   | 20 01  | 01      | 41   | ED   | 66   | 30   | 29.7 °C |
| Temperature 2                 | 604    | 7   | 20 01  | 02      | 41   | EF   | 0D   | B0   | 29.9 °C |
| Request all Measured Supplies | 601    | 2   | 20 02  |         |      |      |      |      |         |
| Backplane +24                 | 604    | 7   | 20 02  | 00      | 41   | BE   | 75   | 98   | 23,8 V  |
| Reserved                      | 604    | 7   | 20 02  | 01      | 00   | 00   | 00   | 00   | 0 (res) |
| Backplane +5                  | 604    | 7   | 20 02  | 02      | 40   | A0   | 51   | EC   | 5,01 V  |
| Reserved                      | 604    | 7   | 20 02  | 03      | 00   | 00   | 00   | 00   | 0 (res) |
| Reserved                      | 604    | 7   | 20 02  | 04      | 00   | 00   | 00   | 00   | 0 (res) |
| Supply +5                     | 604    | 7   | 20 02  | 05      | 40   | 9F   | A2   | 1B   | 4,99 V  |
| Supply +3.3                   | 604    | 7   | 20 02  | 06      | 40   | 53   | 2E   | 1C   | 2,99 V  |
| Reserved                      | 604    | 7   | 20 02  | 07      | 00   | 00   | 00   | 00   | 0 (res) |
| Battery + 24                  | 604    | 7   | 20 02  | 08      | 41   | D0   | CC   | CD   | 26,1 V  |

Table 36



## 3 Commands for High Voltage Devices

### 3.1 General information

Each single HV channel is independently controllable. The modules are software controlled via CAN-Interface through a PC or similar controller.

Using an iseg crate combined with a CC24 controller or an iCSmini as stand alone iseg Communication Server WEB-services, Remote-service, EPICS and SNMP are possible via Ethernet.

We offer a comfortable control programs:

| Control program  | Operating system          | Interfaces    | Protokoll, Standard |
|------------------|---------------------------|---------------|---------------------|
| isegControl2     | Windows, Linux and MAC OS | CAN, Ethernet | EDCP, WS            |
| isegControl1     | Windows and Linux         | CAN, Ethernet | EDCP, OPC DA, SNMP  |
| isegCANHVControl | Windows                   | CAN           | EDCP                |

Table 37: control programs

Using the w-ie-ner Mpod crate it is possible to control up to 10 modules via Ethernet-SNMP Interface.

### 3.2 General settings and options

Please note that there are additional hardware features for these devices in this manual called **OPTION**. The use of an access without the hardware implementation will be described under **OPTION** in manual.

Devices with different bit rate settings do not work on the same CAN bus.

The actual channel and module values (measurement and status) are refreshed approximately every 10ms x number of channels.

The board temperature values are refreshed approximately every 5 up to 10 s.

## 3.3 Operation principle

### 3.3.1 Remote interface control

The communication between an application and the module is performed by the transmission of data items. A data item contains information to be submitted to and/or received from the module. It can represent a specific quantity or a union of single bits. The majority of the data items are standard for all Multi-Channel HV modules and are described in the interface manual in detail. Data items for optional functions are described in the interface options manual.

A general distinction can be made between data items to control individual HV channels and data items to control the HV modules with the sum of all contained channels.

The former group includes the following data items, which exist for every single HV channel:

- items to handle channel status, control and event's
- items to set the voltage or current, bounds, interlock maximum and minimum
- items to read the measured voltage and current
- items to read the nominal voltage and current

The following data items control the properties of the whole HV module. These items exist only once per module:

- items to handle module status, control and events
- voltage ramp speed (is the same for all HV channels)
- current ramp speed (is the same for all HV channels)
- restart time after recalling set values
- maximum set voltage
- maximum set current
- ADC samples per second
- digital filter setting
- power supply voltages
- temperature
- maximum voltage
- maximum current

### 3.3.2 Channel and Module

A high voltage channel is a single high voltage source and measurement circuit. The channel has different operation modes and provides different measurements and status flags.

A module is the combination of one or more high voltage channels in a common housing. Examples are EHS with up to 48 channels. Beside the combination of all channels, the module provides some more measurement and status information for the whole device.

Module commands set a module-wide function or return a module-wide status or measurement value. Channel commands, in contrast, operate on a specific channel. High voltage device operation modes

### 3.3.3 Terminology

| Syntax       | Declaration                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $V_{nom}$    | Voltage nominal, the maximum possible output voltage                                                                                                                                                                                                                                                                                                                                                             |
| $I_{nom}$    | Current nominal, the maximum possible output current                                                                                                                                                                                                                                                                                                                                                             |
| $V_{set}$    | Voltage Set, the user-controllable demanded output voltage                                                                                                                                                                                                                                                                                                                                                       |
| $V_{meas}$   | Voltage Measure, the actual measured output voltage                                                                                                                                                                                                                                                                                                                                                              |
| $V_{lim}$    | Voltage Limit. Can be a hardware or a software limit and serves two purposes: <ol style="list-style-type: none"> <li>1. It limits the upper value of <math>V_{set}</math> to the given limit value: <math> V_{set}  \leq V_{lim}</math></li> <li>2. It generates the Channel Status is Voltage Limit if <math>V_{meas}</math> exceeds the limit value (the exact threshold value is device dependent)</li> </ol> |
| $I_{set}$    | Current Set, the user-controllable demanded output current                                                                                                                                                                                                                                                                                                                                                       |
| $I_{meas}$   | Current Measure, the actual measured output current                                                                                                                                                                                                                                                                                                                                                              |
| $I_{lim}$    | Current Limit. Can be a hardware or a software limit and serves two purposes: <ol style="list-style-type: none"> <li>1. It limits the upper value of <math>I_{set}</math> to the given limit value: <math> I_{set}  \leq I_{lim}</math></li> <li>2. It generates the Channel Status is Current Limit if <math>I_{meas}</math> exceeds the limit value (the exact threshold value is device dependent)</li> </ol> |
| $V_{bounds}$ | Voltage bounds, a tolerance tube $V_{set} \pm V_{bounds}$ around $V_{set}$ . If $V_{meas}$ exceeds this tolerance in either direction, the Channel Status is Voltage Bounds is generated. (condition: no ramping)                                                                                                                                                                                                |
| $I_{bounds}$ | Current bounds, a tolerance tube $I_{set} \pm I_{bounds}$ around $I_{set}$ . If $I_{meas}$ exceeds this tolerance in either direction, the Channel Status is Current Bounds is generated. (condition: no ramping)                                                                                                                                                                                                |

Table 38: Terminology

### 3.3.4 Channel operation modes

| Operation Mode       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Off                  | The channel is off, it does not generate high voltage. If all status conditions are satisfied, the channel can be turned on.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| On                   | The channel is actively generating high voltage.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| Ramping              | The channel ramps to the $V_{set}$ if turned on or is turns off with the programmed ramp speed. EHS FLEX devices provide voltage and current ramp speed setting per channel in V/s resp. A/s. All other devices have a common voltage and current ramp speed for all channels in %/s.                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Emergency Off        | The channel is shut down without ramp. Afterwards, it stays in Emergency Off until Emergency Clear is given.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Emergency Clear      | The channel leaves the state Emergency Off and goes to state Off. If the channel is not in Emergency Off, nothing happens.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Kill Enable active   | The mode Kill Enable provides a higher safety. This mode is module-wide and therefore affects all channels. The channel will got to Trip and shut down without ramp when any of the following conditions occur:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                      | <div><div><div><div><div><math>V_{meas} &gt; V_{lim}</math></div><div><math>I_{meas} &gt; I_{lim}</math></div><div><math>I_{meas} &gt; I_{set}</math></div></div><div>OR</div><div><div><math>V_{meas} &gt; V_{set} + V_{bounds}</math></div><div><math>V_{meas} &lt; V_{set} - V_{bounds}</math></div><div><math>I_{meas} &lt; I_{set} - I_{bounds}</math></div></div></div></div></div>                                                                                                                                                                                                                                                                                                                                                                      |
| Kill Enable inactive | <p>If of the limits above will happen:</p> <ul style="list-style-type: none"><li>Switch the channel from operating mode voltage control into current control if there is a HV hardware with current control.</li><li>HV hardware without current control – a trip in the channel hardware will switch off the high voltage generation. Then the module automatically starts to restore the HV via a voltage ramp to the set voltage. If the HV is held during the trip, e.g. by an external capacity load, the recovery of the HV starts from the voltage at the output. The auto-recovery of the voltage is performed only once in a time span of 10 minutes. If the channel trips a second time within the 10 minutes the HV will be switched off.</li></ul> |
| Constant Voltage     | The channel operates as constant voltage source, that means $V_{meas} \approx V_{set}$ and $I_{meas} < I_{set}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Constant Current     | The channel operates as constant current source, that meas $V_{meas} < V_{set}$ and $I_{meas} \approx I_{set}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Delayed Trip         | This is a special mode of Constant Current. If this mode is activated, and $I_{meas}$ reaches or exceeds $I_{setr}$ , the Channel Status is Current Trip is generated. Depending on the trip configuration, the channel may stay in Constant Current, or turn off with ramp or shut down without ramp. Trip also happens when Kill Enable is active and any of the Kill conditions occur.                                                                                                                                                                                                                                                                                                                                                                      |
| External Inhibit     | <p>External Inhibit is a hardware line to control the high voltage generation. Depending on the device, there might be one External Inhibit per channel or one External Inhibit for all channels. Some devices always shut down the high voltage without ramp on External Inhibit, some devices allow to configure this function.</p> <div><div>External Inhibit individual per channel</div><div>EHS, EHS STACK, NHS and NHR</div><div>External Inhibit is configurable</div><div>EHS, EHS STACK, NHS and NHR</div></div>                                                                                                                                                                                                                                     |
| Input Error          | An input error occurs, if an invalid command or parameter is given, or the parameter of a command exceeds the allowed range. Example: setting a $V_{set}$ of 4000 V for a channel with $V_{nom}$ of 3000 V.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| Output Polarity      | NHR and SHR devices provide switchable output polarities, positive and negative.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| Output Mode          | NHR and SHR devices provide switchable output modes with different voltage and current combinations, e.g. 6kV/1mA and 2kV/3mA.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Voltage Bottom       | EHS Stack provide a special feature to avoid voltage rebound effects that might follow a discharge in GEM detectors.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

Table 39: Channel operation modes

### 3.3.5 Status and Event generation

Channel as well as Module have status and event registers. Both registers contain similar condition bits. The difference between both register types is, that status bits are set and cleared by the device according to the current conditions. Event bits, however, are only set by the device and must be cleared explicitly by the user.

For example, the Status bit is Constant Current indicates that the channel *is now* in constant current mode. The Event bit Event Constant Current in contrast indicates, that the channel has been (or still is) in constant current mode since the last clearing of this bit.

It is thereby possible to clear all status flags at once or to just clear individual bits. In general it is not possible to clear an event bit if the corresponding status bit is still set. The status and event registers are described in detail in section Status and Event registers (3.5 Description of data information per DATA\_ID in EDCP) starts from page 54.

### 3.3.6 Additional current measuring range (Option)

Some modules are equipped with a second current measuring range to capture small current values. The range is automatically detected. In the second range the values will be converted with a higher resolution. The value is in the same floating point format as in the first range. The device control protocol allows to request which range is active.

#### INFORMATION



INFORMATION

The second range cannot be activated if:

- function KillEnable is on.
- a voltage ramp up is running.
- the module operates in CC mode.

## 3.3.7 Control and Status items

### 3.3.7.1 Controls

Control items encapsulate a number of bits which allow to switch On or Off specific functions. There is a control item for the module (ModuleControl) and one for each channel (ChannelControl). Control bits that are used to switch a function permanently are named "set..." (e.g. "setON" to switch a channel On or Off). Bits that initiate the execution of a task just once are named "do..." (e.g. "doClear" to clear all events).

### 3.3.7.2 Status and events

Status items contain a register that encapsulates bits that indicate the current status of the module or channel. Status bits are named starting with "is...". The status always displays only present conditions, if a condition has changed corresponding status bits will be updated.

Unlike the status, event items record previous conditions (e.g. exceeded limits, trips etc.). If an event is registered the corresponding event bit is set permanently to "1" and will keep the information until explicitly reset. Event bits are named starting with "E...".

status Summary of actual condition of module, channel or group

event Event, characterizes a former or actual special condition of module, channel or group

### 3.3.7.3 Event status and event mask

To avoid the need for checking all event sources permanently for incoming events, the module provides a hierarchical chain for the combination of the events to a single status bit. The structure for the event processing allows a combination of events coming from the module status, the status of the channels and the group status. For each event status item a corresponding event mask item is provided. The event mask defines which event status bits contribute to the combined event status.

Event status Events that have been registered so far

Event mask Filter to define which individual events contribute to the summarized event

Between event status items and the corresponding mask is a bit by bit correspondence. The bits in the mask are named starting with "ME...". If the mask bit is set, the occurring of the respective event will activate the combined event. In turn these sum events are collected in an event status register and connected with an event mask register at this higher level.

#### CAUTION!



CAUTION!

If an event bit in the EventStatus is active and the corresponding bit in the EventMask is set, it is not possible to ramp up the voltage or to activate the HV generation if it has been switched off. To unblock this the EventStatus bits must be reset by writing "1" on the corresponding bit positions.

Individual events in the channel event status are starting point of the event combination logic.

First each event status bit for the channel is combined with the corresponding bit in the event mask using a logical AND. Then an event status bit for the channel is generated by combining all resulting bits with a logical OR. The full logical operation is given by

$$\begin{aligned} \text{EventChannelStatus}[n] = & (\text{Channel}[n].\text{EventVoltageLimit AND Channel}[n].\text{MaskEventVoltageLimit}) \text{ OR} \\ & (\text{Channel}[n].\text{EventCurrentLimit AND Channel}[n].\text{MaskEventCurrentLimit}) \text{ OR} \\ & (\text{Channel}[n].\text{EventCurrentTrip AND Channel}[n].\text{MaskEventCurrentTrip}) \text{ OR} \\ & (\text{Channel}[n].\text{EventExtInhibit AND Channel}[n].\text{MaskEventExtInhibit}) \text{ OR} \\ & (\text{Channel}[n].\text{EventVoltageBounds AND Channel}[n].\text{MaskEventVoltageBounds}) \text{ OR} \\ & (\text{Channel}[n].\text{EventCurrentBounds AND Channel}[n].\text{MaskEventCurrentBounds}) \text{ OR} \\ & (\text{Channel}[n].\text{EventCoonstantVoltage AND Channel}[n].\text{MaskEventConstantVoltage}) \text{ OR} \\ & (\text{Channel}[n].\text{EventConstantCurrent AND Channel}[n].\text{MaskEventConstantCurrent}) \text{ OR} \\ & (\text{Channel}[n].\text{EventEmergency AND Channel}[n].\text{MaskEventEmergency}) \text{ OR} \\ & (\text{Channel}[n].\text{EventEndOfRamp AND Channel}[n].\text{MaskEventEndOfRamp}) \text{ OR} \\ & (\text{Channel}[n].\text{EventOnToOff AND Channel}[n].\text{MaskEventOnToOff}) \text{ OR} \\ & (\text{Channel}[n].\text{EventInputError AND Channel}[n].\text{MaskEventInputError}) \end{aligned}$$

The result of the first step for all channels is stored in the register EventChannelStatus.

In the next step all bits of the EventChannelStatus are combined to a single status bit, using the corresponding mask (EventChannelMask). The logical operation is given by

$$\begin{aligned} \text{EventChannelActive} = & (\text{EventChannelStatus}[0] \text{ AND EventChannelMask}[0]) \text{ OR} \\ & (\text{EventChannelStatus}[1] \text{ AND EventChannelMask}[1]) \text{ OR} \\ & \dots \\ & (\text{EventChannelStatus}[n] \text{ AND EventChannelMask}[n]) \end{aligned}$$

A second branch in the event processing logic treats events generated by the status of the module. The following scheme applies to these module events:

$$\begin{aligned} \text{EventModuleActive} = & (\text{EventTemperatureNotGood AND MaskEventTemperatureNotGood}) \text{ OR} \\ & (\text{EventSupplyNotGood AND MaskEventSupplyNotGood}) \text{ OR} \\ & (\text{EventSafetyLoopNotGood AND MaskEventSafetyLoopNotGood}) \end{aligned}$$

A third branch combines events generated by groups (monitor group, timeout group, see chapter 3)

Group events are stored in the status register EventGroupStatus. The mask EventGroupMask is used to generate the combined bit EventGroupActive with the following operation:

$$\begin{aligned} \text{EventGroupActive} = & (\text{EventGroupStatus}[0] \text{ AND EventGroupMask}[0]) \text{ OR} \\ & (\text{EventGroupStatus}[1] \text{ AND EventGroupMask}[1]) \text{ OR} \\ & \dots \\ & (\text{EventGroupStatus}[32] \text{ AND EventGroupMask}[32]) \end{aligned}$$

Finally the three branches are combined to the bit IsEventActive in the register ModuleStatus:

$$\text{IsEventActive} = \text{EventChannelActive OR EventModuleActive OR EventGroupActive}$$

### 3.3.8 Summarizing channel characteristics into groups

The module provides a highly flexible group functionality. A group is a combination of all or a selection of channels with the ability to control or monitor a specified quantity or characteristic of all included channels. There are two classes of groups “Fix Groups” and “Variable Groups”. The former are predefined groups that allow to set single specification values in all channels. The latter are configurable groups that allow to customize the logical structure of the module to the logical structure of the application. They allow an arbitrary assignment of channels and provide a wide range of functionality, structured in four predefined group types. Up to 32 Variable Groups can be defined. The predefined group types are:

#### 3.3.8.1 Set Group

sets a specified channel characteristic in all selected channels

no event generation

#### 3.3.8.2 Status Group

represents the status (condition) of a channel characteristic for all channels

no event generation

#### 3.3.8.3 Monitor Group

monitors the condition of a channel characteristic for selected channels

event generation when the condition changes

configurable response (e.g. switch off)

#### 3.3.8.4 Timeout Group

monitors the current trip in selected channels

to employ this group the signal KillEnable must be turned off

Event generation only after expiry of a predefined time within which the trip condition must be active

configurable response (e.g. switch off)

#### 3.3.8.5 Responses on events (Soft-Kill features)

Event generating groups can be configured to perform one out of four predefined responses if the event has been generated:

- shut down of the whole module without ramp
  - high voltage in all channels of the module is switched off
- switch off all channels that are members of the group without ramp
  - high voltage in all channels of the group is switched off
- switch off all channels that are members of the group with ramp
  - high voltage in all channels of the group is ramped down
- no response
  - no change

## 3.4 Communication via Interface

All modules are controlled via a serial CAN bus interface according to CAN bus specification 2.0A. The actual control protocol is the "Enhanced Device Control Protocol" and is explained more precisely in the following sections.

Furthermore it is implemented a second command set, which corresponds to the deprecated standard protocol "Device Control Protocol". The description of the Device Control Protocol is carried out in the corresponding manual (see 4 Appendix).

We don't recommend to use this data points for actual applications.

### 3.4.1 Enhanced Device Control Protocol EDCP

The communication between the controller and the module is working according to the Enhanced Device Control Protocol EDCP, which has been designed for instruments of Multi-Channel systems by iseg Spezialelektronik GmbH. This protocol is working according to the master slave principle. Therefore, the control of the HV device through a controller in the superior layer is the master in this system, while the module (as a Front-end device with intelligence) is the slave.

The data exchange between the controller and the HV device is working with help of data frames. These data frames are made out of one direction bit DATA\_DIR, one 16bit DATA\_ID and further data bytes. The direction bit DATA\_DIR defines whether the data frame is a write or read-write access. Write access means that the host writes data into the module, read-write access means that the host wants to read data from the module (this is the read access), and the module answers by a write access. The DATA\_ID is characterized through the first bit of the data frame with DATA\_ID.b15=0 of EDCP frames (DATA\_ID.bit7=1 of standard DCP frames). In order to code the type of an access the bit14=1 for a **single channel** access (symbol **S**), bit13=1 for a **group access** (symbol **G**) and bit12=1 for a **module access** (symbol **M**).

The next tables will give an overview of the parts of the EDCP:

| Access                                   | DATA DIR | DATA_ID bits |       |       |       |       |     | CHN bits |      |         |          |
|------------------------------------------|----------|--------------|-------|-------|-------|-------|-----|----------|------|---------|----------|
|                                          |          | Bit15        | Bit14 | Bit13 | Bit12 | Bit11 | ... | Bit1     | Bit0 | Bit7... | ... Bit0 |
| Enhanced DATA_ID                         | 1/0      | 0            | S     | G     | M     |       |     |          |      |         |          |
| Single channel CHN Write access          | 0        | 0            | 1     | 0     | 0     | S11   | ... | S1       | S0   | C7      | C0       |
| Single channel CHN Read-write access     | 1/0      | 0            | 1     | 0     | 0     | S11   | ... | S1       | S0   | C7      | C0       |
| Module Write access                      | 0        | 0            | 0     | 0     | 1     | M11   | ... | M1       | M0   |         |          |
| Module Read-write access                 | 1/0      | 0            | 0     | 0     | 1     | M11   | ... | M1       | M0   |         |          |
| Notes:                                   |          |              |       |       |       |       |     |          |      |         |          |
| S – single channel access                |          |              |       |       |       |       |     |          |      |         |          |
| G – group access                         |          |              |       |       |       |       |     |          |      |         |          |
| M – module access                        |          |              |       |       |       |       |     |          |      |         |          |
| S11 ... S0. – single channel access code |          |              |       |       |       |       |     |          |      |         |          |
| M11 ... M0 – module access code          |          |              |       |       |       |       |     |          |      |         |          |
| C7 ... C0 – Channel multiplex byte CHN   |          |              |       |       |       |       |     |          |      |         |          |

Table 40: parts of the EDCP

If the type of the data frame is a single channel access it will code the corresponding channel information with help of the next multiplex of channel byte (CHN).

If the type of the data frame is a module access then a DATA\_ID is necessary only.

If the type of the data frame is a combination of a single channel and group instruction then it will code the corresponding channel members with help of the next 16bit word (symbol MBR) followed by an OFFSET byte to have a channel start index in steps of 16 (reserved at the moment).

| Access                                                                                                                                                                                                             | DATA DIR | DATA_ID bits |       |       |       |       |     |      |      | CHN / MBR bits  |      | OFFSET               |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|--------------|-------|-------|-------|-------|-----|------|------|-----------------|------|----------------------|
|                                                                                                                                                                                                                    |          | Bit15        | Bit14 | Bit13 | Bit12 | Bit11 | ... | Bit1 | Bit0 | Nmax            | Nmin |                      |
| Enhanced DATA_ID                                                                                                                                                                                                   | 1/0      | 0            | S     | G     | M     |       |     |      |      |                 |      |                      |
| Single channel CHN of members MBR                                                                                                                                                                                  | 1        | 0            | 1     | 1     | 0     | S11   | ... | S1   | S0   | M15 to M0 (MBR) |      | 0, 16 ,32 (reserved) |
| Replay                                                                                                                                                                                                             | 0        |              |       |       |       |       |     |      |      | C47 to C0 (CHN) |      |                      |
| Notes:                                                                                                                                                                                                             |          |              |       |       |       |       |     |      |      |                 |      |                      |
| M15 ... M0 – channel members, every HV channel between 0 and 15 can be added to the request by the corresponding member bit (HV channel 0 will be addressed by M0, HV channel 1 will be addressed by M1 and so on) |          |              |       |       |       |       |     |      |      |                 |      |                      |

Table 41

| INFORMATION                                                                       |                                                                                                                  |
|-----------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|
|  | MBR=0 will address all HV channels of the module, that's is important for modules with more than 16 HV channels. |
| INFORMATION                                                                       |                                                                                                                  |

When a HV device has received such a request message it will answer with multiple CAN frames for all channels which are addressed as members (MBR).

| Access                                 | DATA DIR | DATA_ID bits |       |       |       |     |      |      |  | Data |
|----------------------------------------|----------|--------------|-------|-------|-------|-----|------|------|--|------|
|                                        |          | Bit15        | Bit14 | Bit13 | Bit12 | ... | Bit1 | Bit0 |  |      |
| Group of members MBR Write access      | 0        | 0            | S     | G     | M     | X   | X    |      |  |      |
| Group of members MBR Read-write access | 1        | 0            | 0     | 1     | 0     | G11 | G0   |      |  |      |
|                                        | 0        |              |       |       |       |     |      |      |  |      |

Table 42

The data format of data frame which are coded a group access without a combination of the **S** bit has to be take from the respective description in this manual.

These data frames correspond to a transfer into layer 3 (Network Layer) and layer 4 (Transport Layer) of the OSI model of ISO. The transmission medium is the CAN Bus according to specification 2.0A, related to level1 (Physical Layer) and level 2 (Data Link Layer).

### 3.4.1.1 Data formats

The data format on the network is big endian, i.e. on Intel computers, the value is stored byte-wise reverse. Please use some of the online analysis tools for IEEE-754 floating-point conversion in to the binary format.

|     |                                                     |
|-----|-----------------------------------------------------|
| UI1 | unsigned character                                  |
| SI1 | signed character                                    |
| UI2 | unsigned short integer (16 bit)                     |
| UI4 | unsigned integer (32 bit)                           |
| R4  | float according to IEEE-754 single precision format |

Example Vset:

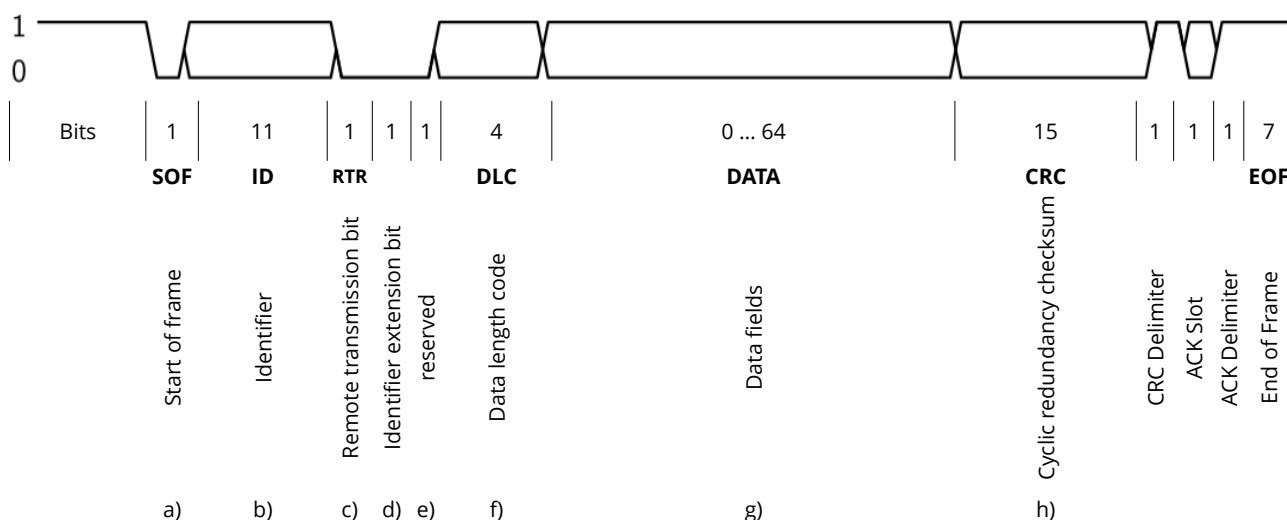
Floating point value = 1000 V:

Binary value in correspondence to IEEE-754 = 0x44 0x7a 0x00 0x00

Data bytes in the big-endian data range of CAN: 0x44 0x7a 0x00 0x00

Data-Bytes in computers using a little endian memory: 0x00 0x00 0x7a 0x44

### 3.4.2 CAN Data Frame



a) Start of frame

b) Identifier

|                   | Bit10 | Bit9 | Bit8  | Bit7  | Bit6  | Bit5  | Bit4  | Bit3  | Bit2 | Bit1 | Bit0     |
|-------------------|-------|------|-------|-------|-------|-------|-------|-------|------|------|----------|
| Front-End Address | 0     | P    | Addr5 | Addr4 | Addr4 | Addr2 | Addr1 | Addr0 | 0    | 0    | DATA_DIR |
| NMT (broadcast)   | 0     | 0    | 0     | 0     | 0     | 0     | 0     | 0     | 1    | 0    | 0        |

Addr5 to Addr0 coding the Front-Address by backplane signals. Please see Appendix E to refer corresponding hardware manuals for more details.

c) Remote transmission bit

d) Identifier extension bit

|                                             |               |
|---------------------------------------------|---------------|
| 11-bit identifiers (EDCP identifiers)       | 0 (dominant)  |
| 29 bit identifiers ((CC24 routing messages) | 1 (recessive) |

e) Reserved

f) 4 bit Data length code (maximum length is 8)

g) Data field

Single channel access: n = 3 to 7 bytes

| DATA ID (n1, n2) | CHANNEL (n3) |           |           |           |          |
|------------------|--------------|-----------|-----------|-----------|----------|
| DATA ID (n1, n2) | CHANNEL (n3) | DATA (n4) | DATA (n5) | DATA (n6) | DATA (7) |

Multiple channel access: n = 5 to 7 bytes

| DATA ID (n1, n2) | Member (n3, n4) | offset (n5) |           |           |          |
|------------------|-----------------|-------------|-----------|-----------|----------|
| DATA ID (n1, n2) | CHANNEL (n3)    | DATA (n4)   | DATA (n5) | DATA (n6) | DATA (7) |

Recommended is member value 0 to requests the DATA\_ID for all channels of the module. Also a request for the first 16 channels can be combined in each case via the member bits (channel 0 by 0x0001, channel1 by 0x0002 and all 16 channels by 0xffff).

offset byte is reserved

Group accesses

|                         |                          |                    |                         |                               |
|-------------------------|--------------------------|--------------------|-------------------------|-------------------------------|
| <b>DATA ID</b> (n1, n2) | <b>Group number</b> (n3) | <b>Offset</b> (n4) |                         |                               |
| <b>DATA ID</b> (n1, n2) | <b>Group number</b> (n3) | <b>Offset</b> (n4) | <b>Members</b> (n5, n6) | <b>Configuration</b> (n6, n7) |

Module access: n = 2 to 6 bytes

|                         |                  |                  |                  |                  |
|-------------------------|------------------|------------------|------------------|------------------|
| <b>DATA ID</b> (n1, n2) |                  |                  |                  |                  |
| <b>DATA ID</b> (n1, n2) | <b>DATA</b> (n3) | <b>DATA</b> (n4) | <b>DATA</b> (n5) | <b>DATA</b> (n6) |

h) 16 bit CRC field = CRC + CRC DelimiterCyclic

Please refer "CAN data link layers in some detail" (Appendix E – Literature references).

Description of Data fields point g)

**DATA ID**

|       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|

The Front-end device must do:

- Processing of NMT services via broadcast messages inside of the CAN segment
- Processing of the single accesses with direct channel values.
- Processing of group information of the module.
- Self-registration in the higher level through sending the module address.
- Building of status information.
- Send an active error message with higher priority if one of the bits - sum status, supply voltages or safety loop - in the group access "General status module" not has been set (the module must be configured as a CAN-node with an Active-CAN message function).

### 3.4.3 Summary of CAN data frame accesses via the NMT service identifier

| Access                                                 | DATA_ DIR | BYTE | NMT DATA_ID Bit |   |    |    |    |    |    |    | read / write / active | DATA-Bytes |
|--------------------------------------------------------|-----------|------|-----------------|---|----|----|----|----|----|----|-----------------------|------------|
|                                                        | ID0       | hex  | 7               | 6 | 5  | 4  | 3  | 2  | 1  | 0  |                       |            |
| No NMT DATA_ID                                         | x         |      | 0               | x | x  | x  | x  | x  | x  | x  |                       |            |
| NMT service CAN segment                                | 0         |      | 1               | 1 | N3 | N2 | N1 | N0 | R1 | R0 |                       |            |
| NMT Address (MICC only)                                | 0/1       | 0x30 | 0               | 0 | 1  | 1  | 0  | 0  | 0  | 0  | w                     | 0/2/3      |
| NMT Start                                              | 0         |      | 1               | 1 | 0  | 0  | 0  | 1  | x  | x  | w                     | 1          |
| NMT Stop                                               | 0         |      | 1               | 1 | 0  | 0  | 1  | 0  | x  | x  | w                     | 1          |
| NMT Reset CAN                                          | 0         |      | 1               | 1 | 0  | 0  | 1  | 1  | x  | x  | w                     | 1          |
| NMT Reset hardware                                     | 0         |      | 1               | 1 | 0  | 1  | 0  | 0  | x  | x  | w                     | 1          |
| NMT set of Bit rate                                    | 0         |      | 1               | 1 | 0  | 1  | 0  | 1  | x  | x  | w                     | 3          |
| NMT set of temperature                                 | 0         |      | 1               | 1 | 0  | 1  | 1  | 0  | x  | x  | w                     | 3          |
| NMT mode set                                           | 0         |      | 1               | 1 | 1  | 0  | 0  | 0  | x  | x  | w                     | 2/6        |
| NMT set standard DCP or enhanced DCP                   | 0         |      | 1               | 1 | 1  | 0  | 0  | 1  | x  | x  | w                     | 2          |
| NMT channel group set                                  | 0         |      | 1               | 1 | 1  | 0  | 1  | 0  | x  | x  | w                     | 8/6        |
| NMT module set                                         | 0         |      | 1               | 1 | 1  | 0  | 1  | 1  | x  | x  | w                     | 8/6        |
| Notes:<br>N3 ... N0: NMT access<br>R1 ... R0: reserved |           |      |                 |   |    |    |    |    |    |    |                       |            |

Table 43: Summary of CAN data frame

NMT Address (MICC only)

| Access                   | CAN ID (NMT) | RTR | EXT_INSTR | DATA_DIR | DATA_ID | DATA_1      | DATA_0      |
|--------------------------|--------------|-----|-----------|----------|---------|-------------|-------------|
| NMT-RTR master           | 0x004        | 1   | 0         | 0        | -       | -           | -           |
| NMT-RTR board reply      | 0x003        | 0   | 0         | 0        | 0xC0    | address     | -           |
| NMT Address master write | 0x004        | 0   | 0         | 0        | 0xC0    | old address | new address |

Table 44

|                        |                                                                                                                                                                                                     |
|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NMT Start              | The state of all Front-end devices is going to OPERATIONAL (see 4.2 Appendix B – Diagram of operating modes)                                                                                        |
| NMT Stop               | The state of all Front-end devices is going to PREPARED<br>This is necessary before storing any information permanently in EEPROM or execute one of the following NMT services.                     |
| NMT Reset CAN          | re - initialise all connected iseg Multi-Channel CAN devices.                                                                                                                                       |
| NMT Reset hardware     | execute a hardware reset of all connected CAN devices.                                                                                                                                              |
| NMT set of Bit rate    | set a new bit rate for all connected iseg Multi-Channel CAN devices (DATA_1 / DATA_0 see group access <a href="#">Bit rate</a> , chapter 3.5.2.25 Bit rate (module write- / read-write access))     |
| NMT set of temperature | An offset for the calculation of the temperature will be calculated in all modules which receive this message. DATA_1 to DATA_0 contains the measured temperature in tenth parts of °C as UI2 type. |

|        |        |
|--------|--------|
| DATA_1 | DATA_0 |
| MSB    | LSB    |

#### NMT mode set

| Mode                | Data_0    | Description                                        |
|---------------------|-----------|----------------------------------------------------|
| NORMAL_MODE         | 000       | Operating Mode "Operational" without any condition |
| FACTORY MODES       | 001 - 005 | will used in production of the modules only!       |
| LIVE_INSERTION_MODE | 006       | Mode to avoid events during a live insertion       |

Table 45: NMT mode set

|                                       |                       |      |
|---------------------------------------|-----------------------|------|
| NMT set standard DCP or enhanced DCP: | DATA_0=0 standard DCP | DCP  |
|                                       | DATA_0=1 enhanced DCP | EDCP |

#### NMT broadcast messages

#### NMT channel group set frame:

| Access                   | DATA_DIR | NMT DATA_ID | GROUP | EDCP DATA_ID | EDCP Multiple Single Channels Access | DATAn            | DATAn-1 | DATAn-2 | DATAn-3 |
|--------------------------|----------|-------------|-------|--------------|--------------------------------------|------------------|---------|---------|---------|
| NMT group voltage set    | 0        | 0xe8        | Group | 0x6100       |                                      | Voltage [R4]     |         |         |         |
| NMT group current set    | 0        | 0xe8        | Group | 0x6101       |                                      | Current [R4]     |         |         |         |
| NMT group control set    | 0        | 0xe8        | Group | 0x6001       |                                      | Control [UI2]    |         |         |         |
| NMT group event mask set | 0        | 0xe8        | Group | 0x6003       |                                      | Event mask [UI2] |         |         |         |

Table 46: NMT channel group set

Group 0..255 (group = 0 after power on of the module)

NMT module set frame:

| Access                     | DATA_DIR | NMT DATA_ID | GROUP    | EDCP DATA_ID EDCP Module Access | DATAn                   |
|----------------------------|----------|-------------|----------|---------------------------------|-------------------------|
| NMT voltage ramp speed set | 0        | 0xec        | reserved | 0x1100                          | Voltage ramp speed [R4] |
| NMT current ramp speed set | 0        | 0xec        | reserved | 0x1101                          | Current ramp speed [R4] |
| NMT control set            | 0        | 0xec        | reserved | 0x1001                          | Control [UI2]           |
| NMT event mask             | 0        | 0xec        | reserved | 0x1003                          | Event mask [UI2]        |
| NMT event channel mask     | 0        | 0xec        | reserved | 0x1005                          | Event mask [UI2]        |

Table 47: NMT module set

With one of the NMT channel group set or the NMT module set frames a message is sent to the corresponding data point of the table above in kind of a broadcast information for all channels, which have the same group number GROUP. The detailed description of the frames can be found by a click on the arrows of the tables. The EDCP Single Channel Access [GroupNumber](#) (described on 3.5.1.43 Group number (single/ multiple single read-write access)) handles the distribution of a group number for each channel.

Example: Switch ON all channels of the whole system (group number after reset of all channels is zero)

| ID    | DLC | NMT DATA_ID | GROUP | EDCP DATA_ID Multiple Single Channel Access | Channel control |
|-------|-----|-------------|-------|---------------------------------------------|-----------------|
| 0x004 | 0x6 | 0xe6        | 0x00  | 0x6001                                      | 0x0008          |

Table 48

### 3.4.4 Summary of CAN data frame accesses via the Front-end-address identifier

Multi-channel High Voltage CAN modules are made out of one or two PCBs (in order to double the number of HV channels) and one digital CAN Interface per PCB.

Each module board has to be controlled separately via its own CAN nodes identifier (see 3.4.2 CAN Data Frame to control the HV modules above).

#### 3.4.4.1 List to access of the EDCP made for HV boards up to 255 channels EDCP Single Channel Accesses

| Access                       | DATA_DIR   | WORD          | DATA_ID Bit |          |          |          |                                 |                  |                  |                  |                  |     | read / write / active | DATA Bytes | Page |
|------------------------------|------------|---------------|-------------|----------|----------|----------|---------------------------------|------------------|------------------|------------------|------------------|-----|-----------------------|------------|------|
|                              | ID0        | hex           | 15          | 14       | 13       | 12       | 11                              | ...              | ...              | 1                | 0                |     |                       |            |      |
| DATA_ID                      |            |               | 0           | S        | G        | M        | x <sup>(2)</sup>                | x <sup>(2)</sup> | x <sup>(2)</sup> | x <sup>(2)</sup> | x <sup>(2)</sup> |     |                       |            |      |
| <b>Single channel access</b> | <b>1/0</b> | <b>0x4xxx</b> | <b>0</b>    | <b>1</b> | <b>0</b> | <b>0</b> | <b>S11 ... S0<sup>(1)</sup></b> |                  |                  |                  |                  |     |                       |            |      |
| ChannelStatus                | 1          | 0x4000        | 0           | 1        | 0        | 0        | 0x000                           |                  |                  |                  |                  | r   | 3/5                   | 54         |      |
| ChannelStatus32              | 1          | 0x4080        | 0           | 1        | 0        | 0        | 0x080                           |                  |                  |                  |                  | r   | 3/7                   | 54         |      |
| ChannelControl               | 1/0        | 0x4001        | 0           | 1        | 0        | 0        | 0x001                           |                  |                  |                  |                  | r/w | 3/5                   | 57         |      |
| ChannelControl32             | 1/0        | 0x4081        | 0           | 1        | 0        | 0        | 0x081                           |                  |                  |                  |                  | r/w | 3/7                   | 57         |      |
| ChannelEventStatus           | 1/0        | 0x4002        | 0           | 1        | 0        | 0        | 0x002                           |                  |                  |                  |                  | r/w | 3/5                   | 58         |      |
| ChannelEventStatus32         | 1/0        | 0x4082        | 0           | 1        | 0        | 0        | 0x082                           |                  |                  |                  |                  | r/w | 3/7                   | 59         |      |
| ChannelEventMask             | 1/0        | 0x4003        | 0           | 1        | 0        | 0        | 0x003                           |                  |                  |                  |                  | r/w | 3/5                   | 61         |      |
| ChannelEventMask             | 1/0        | 0x4083        | 0           | 1        | 0        | 0        | 0x083                           |                  |                  |                  |                  | r/w | 3/7                   | 61         |      |
| DelayedTripTime              | 1/0        | 0x4005        | 0           | 1        | 0        | 0        | 0x005                           |                  |                  |                  |                  | r/w | 3/5                   | 63         |      |
| DelayedTripAction            | 1/0        | 0x4006        | 0           | 1        | 0        | 0        | 0x006                           |                  |                  |                  |                  | r/w | 3/4                   | 63         |      |
| ExternalInhibitAction        | 1/0        | 0x4007        | 0           | 1        | 0        | 0        | 0x007                           |                  |                  |                  |                  | r/w | 3/4                   | 64         |      |
| VoltageRampPriority          | 1/0        | 0x4010        | 0           | 1        | 0        | 0        | 0x010                           |                  |                  |                  |                  | r/w | 3/5                   | 64         |      |
| VoltageSet                   | 1/0        | 0x4100        | 0           | 1        | 0        | 0        | 0x100                           |                  |                  |                  |                  | r/w | 3/7                   | 65         |      |
| CurrentSet / CurrentTrip     | 1/0        | 0x4101        | 0           | 1        | 0        | 0        | 0x101                           |                  |                  |                  |                  | r/w | 3/7                   | 65         |      |
| VoltageMeasure               | 1          | 0x4102        | 0           | 1        | 0        | 0        | 0x102                           |                  |                  |                  |                  | r   | 3/7                   | 66         |      |
| CurrentMeasure               | 1          | 0x4103        | 0           | 1        | 0        | 0        | 0x103                           |                  |                  |                  |                  | r   | 3/7                   | 66         |      |
| VoltageBounds                | 1/0        | 0x4104        | 0           | 1        | 0        | 0        | 0x104                           |                  |                  |                  |                  | r/w | 3/7                   | 67         |      |
| CurrentBounds                | 1/0        | 0x4105        | 0           | 1        | 0        | 0        | 0x105                           |                  |                  |                  |                  | r/w | 3/7                   | 67         |      |
| VoltageNominal               | 1          | 0x4106        | 0           | 1        | 0        | 0        | 0x106                           |                  |                  |                  |                  | r   | 3/7                   | 68         |      |
| CurrentNominal               | 1          | 0x4107        | 0           | 1        | 0        | 0        | 0x107                           |                  |                  |                  |                  | r   | 3/7                   | 68         |      |
| <u>PowerNominal</u>          | 1          | 0x4108        | 0           | 1        | 1        | 0        | 0x108                           |                  |                  |                  |                  | r   | 3/7                   | 68         |      |
| CurrentMeasure Range         | 1          | 0x4109        | 0           | 1        | 0        | 0        | 0x109                           |                  |                  |                  |                  | r   | 3/8                   | 69         |      |
| VoltageBottom                | 1/0        | 0x410A        | 0           | 1        | 0        | 0        | 0x10A                           |                  |                  |                  |                  | r/w | 3/7                   | 69         |      |
| VctCoefficient               | 1/0        | 0x4120        | 0           | 1        | 0        | 0        | 0x120                           |                  |                  |                  |                  | r/w | 3/7                   | 70         |      |
| TemperatureExternal          | 1          | 0x4121        | 0           | 1        | 0        | 0        | 0x121                           |                  |                  |                  |                  | r/w | 3/7                   | 70         |      |
| ResistorExternal             | 1/0        | 0x4122        | 0           | 1        | 0        | 0        | 0x122                           |                  |                  |                  |                  | r/w | 3/7                   | 71         |      |
| VoltageRampSpeedUp           | 1/0        | 0x4123        | 0           | 1        | 0        | 0        | 0x123                           |                  |                  |                  |                  | r/w | 3/7                   | 71         |      |
| VoltageRampSpeedDown         | 1/0        | 0x4124        | 0           | 1        | 0        | 0        | 0x124                           |                  |                  |                  |                  | r/w | 3/7                   | 72         |      |

| Access                                                                                                                                                                                                                                                                                             | DATA_DIR | WORD   | DATA_ID Bit |   |   |   |       | read / write / active | DATA Bytes | Page |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|--------|-------------|---|---|---|-------|-----------------------|------------|------|
| CurrentRampSpeedUp                                                                                                                                                                                                                                                                                 | 1/0      | 0x4125 | 0           | 1 | 0 | 0 | 0x125 | r/w                   | 3/7        | 72   |
| CurrentRampSpeedDown                                                                                                                                                                                                                                                                               | 1/0      | 0x4126 | 0           | 1 | 0 | 0 | 0x126 | r/w                   | 3/7        | 73   |
| VoltageRampSpeedMin                                                                                                                                                                                                                                                                                | 1/0      | 0x4127 | 0           | 1 | 0 | 0 | 0x127 | r/w                   | 3/7        | 73   |
| VoltageRampSpeedMax                                                                                                                                                                                                                                                                                | 1/0      | 0x4128 | 0           | 1 | 0 | 0 | 0x128 | r/w                   | 3/7        | 74   |
| CurrentRampSpeedMin                                                                                                                                                                                                                                                                                | 1/0      | 0x4129 | 0           | 1 | 0 | 0 | 0x129 | r/w                   | 3/7        | 74   |
| CurrentRampSpeedMax                                                                                                                                                                                                                                                                                | 1/0      | 0x4130 | 0           | 1 | 0 | 0 | 0x130 | r/w                   | 3/7        | 75   |
| <u>PowerSet</u>                                                                                                                                                                                                                                                                                    | 1/0      | 0x4134 | 0           | 1 | 0 | 0 | 0x134 | r/w                   | 3/7        | 75   |
| <u>PowerMeasure</u>                                                                                                                                                                                                                                                                                | 1        | 0x4135 | 0           | 1 | 0 | 0 | 0x135 | r                     | 3/7        | 76   |
| OutputMode                                                                                                                                                                                                                                                                                         | 1/0      | 0x4140 | 0           | 1 | 0 | 0 | 0x140 | r/w                   | 3/4        | 76   |
| OutputPolarity                                                                                                                                                                                                                                                                                     | 1/0      | 0x4141 | 0           | 1 | 0 | 0 | 0x141 | r/w                   | 3/4        | 77   |
| VoltageMode                                                                                                                                                                                                                                                                                        | 1        | 0x4142 | 0           | 1 | 0 | 0 | 0x142 | r                     | 3/7        | 77   |
| CurrentMode                                                                                                                                                                                                                                                                                        | 1        | 0x4143 | 0           | 1 | 0 | 0 | 0x143 | r                     | 3/7        | 78   |
| <u>VoltageModeList</u>                                                                                                                                                                                                                                                                             | 1        | 0x4150 | 0           | 1 | 0 | 0 | 0x150 | r                     | 3/7        | 78   |
| <u>CurrentModeList</u>                                                                                                                                                                                                                                                                             | 1        | 0x4160 | 0           | 1 | 0 | 0 | 0x160 | r                     | 3/7        | 78   |
| <u>GroupNumber</u>                                                                                                                                                                                                                                                                                 | 1/0      | 0x4200 | 0           | 1 | 0 | 0 | 0x200 | r/w                   | 3/4        | 79   |
| Notes:<br>S DATA_ID type bit for a EDCP-frame of an access to a single channel<br>G DATA_ID type bit for a EDCP-frame of an access to a group of channels<br>M DATA_ID type bit for a EDCP-frame of an access to the whole module<br>1) Sn single channel access bits, (n=0 ... 11)<br>2) x 0 or 1 |          |        |             |   |   |   |       |                       |            |      |

Table 49: List to access of the EDCP

### 3.4.4.2 EDCP Multiple Single Channels Access

| Access                       | DATA_DIR | WORD          | DATA_ID Bit |          |          |          |                                 |                  |                  |                  |                  |   |  | read / write / active | DATA Bytes | Page |
|------------------------------|----------|---------------|-------------|----------|----------|----------|---------------------------------|------------------|------------------|------------------|------------------|---|--|-----------------------|------------|------|
|                              | ID0      | hex           | 15          | 14       | 13       | 12       | ...                             | ...              | ...              | 1                | 0                |   |  |                       |            |      |
| <b>DATA_ID</b>               |          |               | <b>0</b>    | <b>S</b> | <b>G</b> | <b>M</b> | x <sup>(2)</sup>                | x <sup>(2)</sup> | x <sup>(2)</sup> | x <sup>(2)</sup> | x <sup>(2)</sup> |   |  |                       |            |      |
| <b>Single channel access</b> | <b>1</b> | <b>0x6xxx</b> | <b>0</b>    | <b>1</b> | <b>1</b> | <b>0</b> | <b>S11 ... S0<sup>(1)</sup></b> |                  |                  |                  |                  |   |  |                       |            |      |
| ChannelStatus                | 1        | 0x6000        | 0           | 1        | 1        | 0        | 0x000                           |                  |                  |                  |                  | r |  | 5/5                   | 54         |      |
| ChannelStatus32              | 1        | 0x6080        | 0           | 1        | 1        | 0        | 0x080                           |                  |                  |                  |                  | r |  | 5/7                   | 54         |      |
| ChannelControl               | 1        | 0x6001        | 0           | 1        | 0        | 0        | 0x001                           |                  |                  |                  |                  | r |  | 5/5                   | 57         |      |
| ChannelControl32             | 1        | 0x6081        | 0           | 1        | 0        | 0        | 0x081                           |                  |                  |                  |                  | r |  | 5/7                   | 57         |      |
| ChannelEventStatus           | 1        | 0x6002        | 0           | 1        | 1        | 0        | 0x002                           |                  |                  |                  |                  | r |  | 5/5                   | 58         |      |
| ChannelEventStatus32         | 1        | 0x6082        | 0           | 1        | 1        | 0        | 0x082                           |                  |                  |                  |                  | r |  | 5/7                   | 59         |      |
| ChannelEventMask             | 1        | 0x6003        | 0           | 1        | 1        | 0        | 0x003                           |                  |                  |                  |                  | r |  | 5/5                   | 61         |      |
| ChannelEventMask32           | 1        | 0x6083        | 0           | 1        | 1        | 0        | 0x083                           |                  |                  |                  |                  | r |  | 5/7                   | 61         |      |
| DelayedTripTime              | 1        | 0x6005        | 0           | 1        | 1        | 0        | 0x005                           |                  |                  |                  |                  | r |  | 5/5                   | 63         |      |
| DelayedTripAction            | 1        | 0x6006        | 0           | 1        | 1        | 0        | 0x006                           |                  |                  |                  |                  | r |  | 5/4                   | 63         |      |
| ExternalInhibitAction        | 1        | 0x6007        | 0           | 1        | 1        | 0        | 0x007                           |                  |                  |                  |                  | r |  | 5/4                   | 64         |      |
| VoltageRampPriority          | 1        | 0x6010        | 0           | 1        | 1        | 0        | 0x010                           |                  |                  |                  |                  | r |  | 5/5                   | 64         |      |
| VoltageSet                   | 1        | 0x6100        | 0           | 1        | 1        | 0        | 0x100                           |                  |                  |                  |                  | r |  | 5/7                   | 65         |      |
| CurrentSet / CurrentTrip     | 1        | 0x6101        | 0           | 1        | 1        | 0        | 0x101                           |                  |                  |                  |                  | r |  | 5/7                   | 65         |      |
| VoltageMeasure               | 1        | 0x6102        | 0           | 1        | 1        | 0        | 0x102                           |                  |                  |                  |                  | r |  | 5/7                   | 66         |      |
| CurrentMeasure               | 1        | 0x6103        | 0           | 1        | 1        | 0        | 0x103                           |                  |                  |                  |                  | r |  | 5/7                   | 66         |      |
| VoltageBounds                | 1        | 0x6104        | 0           | 1        | 1        | 0        | 0x104                           |                  |                  |                  |                  | r |  | 5/7                   | 67         |      |
| CurrentBounds                | 1        | 0x6105        | 0           | 1        | 1        | 0        | 0x105                           |                  |                  |                  |                  | r |  | 5/7                   | 67         |      |
| VoltageNominal               | 1        | 0x6106        | 0           | 1        | 1        | 0        | 0x106                           |                  |                  |                  |                  | r |  | 5/7                   | 68         |      |
| CurrentNominal               | 1        | 0x6107        | 0           | 1        | 1        | 0        | 0x107                           |                  |                  |                  |                  | r |  | 5/7                   | 68         |      |
| <u>PowerNominal</u>          | 1        | 0x6108        | 0           | 1        | 1        | 0        | 0x108                           |                  |                  |                  |                  | r |  | 5/7                   | 68         |      |
| CurrentMeasure Range         | 1        | 0x6109        | 0           | 1        | 1        | 0        | 0x109                           |                  |                  |                  |                  | r |  | 5/8                   | 69         |      |
| VoltageBottom                | 1        | 0x610A        | 0           | 1        | 1        | 0        | 0x10A                           |                  |                  |                  |                  | r |  | 5/7                   | 69         |      |
| VctCoefficient               | 1        | 0x6120        | 0           | 1        | 1        | 0        | 0x120                           |                  |                  |                  |                  | r |  | 5/7                   | 70         |      |
| TemperatureExternal          | 1        | 0x6121        | 0           | 1        | 1        | 0        | 0x121                           |                  |                  |                  |                  | r |  | 5/7                   | 70         |      |
| ResistorExternal             | 1        | 0x6122        | 0           | 1        | 1        | 0        | 0x122                           |                  |                  |                  |                  | r |  | 5/7                   | 71         |      |
| VoltageRampSpeedUp           | 1        | 0x6123        | 0           | 1        | 0        | 0        | 0x123                           |                  |                  |                  |                  | r |  | 5/7                   | 71         |      |
| VoltageRampSpeedDown         | 1        | 0x6124        | 0           | 1        | 0        | 0        | 0x124                           |                  |                  |                  |                  | r |  | 3/7                   | 72         |      |
| CurrentRampSpeedUp           | 1        | 0x6125        | 0           | 1        | 0        | 0        | 0x125                           |                  |                  |                  |                  | r |  | 3/7                   | 72         |      |
| CurrentRampSpeedDown         | 1        | 0x6126        | 0           | 1        | 0        | 0        | 0x126                           |                  |                  |                  |                  | r |  | 3/7                   | 73         |      |
| VoltageRampSpeedMin          | 1        | 0x6127        | 0           | 1        | 0        | 0        | 0x127                           |                  |                  |                  |                  | r |  | 3/7                   | 73         |      |
| VoltageRampSpeedMax          | 1        | 0x6128        | 0           | 1        | 0        | 0        | 0x128                           |                  |                  |                  |                  | r |  | 3/7                   | 74         |      |
| CurrentRampSpeedMin          | 1        | 0x6129        | 0           | 1        | 0        | 0        | 0x129                           |                  |                  |                  |                  | r |  | 3/7                   | 74         |      |
| CurrentRampSpeedMax          | 1        | 0x6130        | 0           | 1        | 0        | 0        | 0x130                           |                  |                  |                  |                  | r |  | 3/7                   | 75         |      |

| Access                                                                                                                                                                                                                                                                                           | DATA_DIR | WORD   | DATA_ID Bit |   |   |   |       | read / write / active | DATA Bytes | Page |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|--------|-------------|---|---|---|-------|-----------------------|------------|------|
| PowerSet                                                                                                                                                                                                                                                                                         | 1        | 0x6134 | 0           | 1 | 0 | 0 | 0x134 | r/w                   | 3/7        | 75   |
| PowerMeasure                                                                                                                                                                                                                                                                                     | 1        | 0x6135 | 0           | 1 | 0 | 0 | 0x135 | r                     | 3/7        | 76   |
| OutputMode                                                                                                                                                                                                                                                                                       | 1        | 0x6140 | 0           | 1 | 1 | 0 | 0x140 | r                     | 3/4        | 76   |
| OutputPolarity                                                                                                                                                                                                                                                                                   | 1        | 0x6141 | 0           | 1 | 1 | 0 | 0x141 | r                     | 5/4        | 77   |
| VoltageMode                                                                                                                                                                                                                                                                                      | 1        | 0x6142 | 0           | 1 | 1 | 0 | 0x142 | r                     | 5/7        | 77   |
| CurrentMode                                                                                                                                                                                                                                                                                      | 1        | 0x6143 | 0           | 1 | 1 | 0 | 0x143 | r                     | 5/7        | 78   |
| VoltageModeList                                                                                                                                                                                                                                                                                  | 1        | 0x6150 | 0           | 1 | 1 | 0 | 0x150 | r                     | 5/7        | 78   |
| CurrentModeList                                                                                                                                                                                                                                                                                  | 1        | 0x6160 | 0           | 1 | 1 | 0 | 0x150 | r                     | 5/7        | 78   |
| ChannelGroup                                                                                                                                                                                                                                                                                     | 1        | 0x6200 | 0           | 1 | 1 | 0 | 0x200 | r                     | 6          | 79   |
| Notes:<br>S DATA_ID type bit for a EDCP-frame of an access to single channel<br>G DATA_ID type bit for a EDCP-frame of an access to a group of channels<br>M DATA_ID type bit for a EDCP-frame of an access to the whole module<br>1) Sn single channel access bits, (n=0 ... 11)<br>2) x 0 or 1 |          |        |             |   |   |   |       |                       |            |      |

Table 50: EDCP Multiple Single Channels Access

### 3.4.4.3 Module Access

| Access                     | DATA_ DIR  | WORD          | DATA_ID Bit |          |          |          |                                 |                  |                  |                  |                  |     | read / write / active | DATA-Bytes | Page |
|----------------------------|------------|---------------|-------------|----------|----------|----------|---------------------------------|------------------|------------------|------------------|------------------|-----|-----------------------|------------|------|
|                            | ID0        | hex           | 15          | 14       | 13       | 12       | ...                             | ...              | ...              | 1                | 0                |     |                       |            |      |
| <b>DATA_ID</b>             |            |               | <b>0</b>    | <b>S</b> | <b>G</b> | <b>M</b> | x <sup>(2)</sup>                | x <sup>(2)</sup> | x <sup>(2)</sup> | x <sup>(2)</sup> | x <sup>(2)</sup> |     |                       |            |      |
| <b>Module access</b>       | <b>1/0</b> | <b>0x1xxx</b> | <b>0</b>    | <b>0</b> | <b>0</b> | <b>1</b> | <b>M11 ... M0<sup>(1)</sup></b> |                  |                  |                  |                  |     |                       |            |      |
| ModuleStatus               | 1          | 01000         | 0           | 0        | 0        | 1        | 0x000                           |                  |                  |                  |                  | r   | 2/4                   | 79         |      |
| ModuleStatus32             | 1          | 01080         | 0           | 0        | 0        | 1        | 0x080                           |                  |                  |                  |                  | r   | 2/6                   | 80         |      |
| ModuleControl              |            | 0x1001        | 0           | 0        | 0        | 1        | 0x001                           |                  |                  |                  |                  | r/w | 2/4                   | 83         |      |
| ModuleControl32            |            | 0x1081        | 0           | 0        | 0        | 1        | 0x081                           |                  |                  |                  |                  | r/w | 2/6                   | 83         |      |
| ModuleEventStatus          | 1/0        | 0x1002        | 0           | 0        | 0        | 1        | 0x002                           |                  |                  |                  |                  | r/w | 2/4                   | 85         |      |
| ModuleEventStatus32        | 1/0        | 0x1082        | 0           | 0        | 0        | 1        | 0x082                           |                  |                  |                  |                  | r/w | 2/6                   | 85         |      |
| ModuleEventMask            | 1/0        | 0x1003        | 0           | 0        | 0        | 1        | 0x003                           |                  |                  |                  |                  | r/w | 2/4                   | 86         |      |
| ModuleEventMask32          | 1/0        | 0x1083        | 0           | 0        | 0        | 1        | 0x083                           |                  |                  |                  |                  | r/w | 2/6                   | 87         |      |
| ModuleEventChannelStatus   | 1/0        | 0x1004        | 0           | 0        | 0        | 1        | 0x004                           |                  |                  |                  |                  | r/w | 2/4                   | 88         |      |
| ModuleEventChannelStatus32 | 1/0        | 0x1084        | 0           | 0        | 0        | 1        | 0x084                           |                  |                  |                  |                  | r/w | 2/6                   | 88         |      |
| ModuleEventChannelMask     | 1/0        | 0x1005        | 0           | 0        | 0        | 1        | 0x005                           |                  |                  |                  |                  | r/w | 2/4                   | 89         |      |
| ModuleEventChannelMask32   | 1/0        | 0x1085        | 0           | 0        | 0        | 1        | 0x085                           |                  |                  |                  |                  | r/w | 2/6                   | 89         |      |
| ModuleEventGroupStatus     | 1/0        | 0x1006        | 0           | 0        | 0        | 1        | 0x006                           |                  |                  |                  |                  | r/w | 2/4                   | 90         |      |
| ModuleEventGroupMask       | 1/0        | 0x1007        | 0           | 0        | 0        | 1        | 0x007                           |                  |                  |                  |                  | r/w | 4/2                   | 91         |      |
| VoltageRampSpeed           | 1/0        | 0x1100        | 0           | 0        | 0        | 1        | 0x100                           |                  |                  |                  |                  | r/w | 2/6                   | 92         |      |
| CurrentRampSpeed           | 1/0        | 0x1101        | 0           | 0        | 0        | 1        | 0x101                           |                  |                  |                  |                  | r/w | 2/6                   | 92         |      |
| VoltageMax                 | 1          | 0x1102        | 0           | 0        | 0        | 1        | 0x102                           |                  |                  |                  |                  | r   | 2/6                   | 93         |      |
| CurrentMax                 | 1          | 0x1103        | 0           | 0        | 0        | 1        | 0x103                           |                  |                  |                  |                  | r   | 2/6                   | 94         |      |
| Supply24                   | 1          | 0x1104        | 0           | 0        | 0        | 1        | 0x104                           |                  |                  |                  |                  | r   | 2/6                   | 94         |      |
| Supply5                    | 1          | 0x1105        | 0           | 0        | 0        | 1        | 0x105                           |                  |                  |                  |                  | r   | 2/6                   | 95         |      |
| BoardTemperature           | 1          | 0x1106        | 0           | 0        | 0        | 1        | 0x106                           |                  |                  |                  |                  | r   | 2/6                   | 95         |      |
| ThresholdArmErrorDetection | 1/0        | 0x1107        | 0           | 0        | 0        | 1        | 0x107                           |                  |                  |                  |                  | r/w | 2/6                   | 95         |      |
| SerialNumber               | 1          | 0x1200        | 0           | 0        | 0        | 1        | 0x200                           |                  |                  |                  |                  | r   | 2/6                   | 95         |      |
| FirmwareRelease            | 1          | 0x1201        | 0           | 0        | 0        | 1        | 0x201                           |                  |                  |                  |                  | r   | 2/6                   | 96         |      |
| BitRate                    | 0/1        | 0x1202        | 0           | 0        | 0        | 1        | 0x202                           |                  |                  |                  |                  | r   | 4/2                   | 96         |      |
| NameOfFirmware             | 1          | 0x1203        | 0           | 0        | 0        | 1        | 0x203                           |                  |                  |                  |                  | r   | 5/6                   | 97         |      |
| ADC SamplesPerSecond       | 1/0        | 0x1204        | 0           | 0        | 0        | 1        | 0x204                           |                  |                  |                  |                  | r/w | 4/2                   | 98         |      |
| DigitalFilter              | 1/0        | 0x1205        | 0           | 0        | 0        | 1        | 0x205                           |                  |                  |                  |                  | r/w | 4/2                   | 98         |      |

| Access                                                                                                                                                                                                                                                                                                         | DATA_ DIR | WORD   | DATA_ID Bit |   |   |   |       | read / write / active | DATA- Bytes | Page |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------|-------------|---|---|---|-------|-----------------------|-------------|------|
| ChannelNumber                                                                                                                                                                                                                                                                                                  | 1         | 0x1208 | 0           | 0 | 0 | 1 | 0x208 | r                     | 6           | 98   |
| ArticleDescription                                                                                                                                                                                                                                                                                             | 1         | 0x1209 | 0           | 0 | 0 | 1 | 0x209 | r                     | 8           | 98   |
| ModuleOption                                                                                                                                                                                                                                                                                                   | 1         | 0x1280 | 0           | 0 | 0 | 1 | 0x280 | r                     | 6           | 99   |
| ModuleOptionSpec                                                                                                                                                                                                                                                                                               | 1         | 0x1290 | 0           | 0 | 0 | 1 | 0x290 | r                     | 7           | 101  |
| ModuleCommMode                                                                                                                                                                                                                                                                                                 | 0         | 0x12A0 | 0           | 0 | 0 | 1 | 0x2A0 | w                     | 4           | 102  |
| FactorySettings                                                                                                                                                                                                                                                                                                | 1/0       | 0x1401 | 0           | 0 | 0 | 1 | 0x401 | r/w                   | 4/8         | -    |
| Notes:<br>S DATA_ID type bit for a EDCP-frame of an access to single channel<br>G DATA_ID type bit for a EDCP-frame of an access to a group of channels<br>M DATA_ID type bit for a EDCP-frame of an access to the whole module<br><sup>1)</sup> Mn module access bits, (n=0 ... 11)<br><sup>2)</sup> x 0 or 1 |           |        |             |   |   |   |       |                       |             |      |

Table 51: Module Access

### 3.4.4.4 EDCP Group Accesses

| Access                                | DATA_ DIR                                                             | WORD                            | DATA_ID Bit |    |    |    |                  |                  |                  |                  |                  |     | read / write / active | DATA- Bytes | Page |
|---------------------------------------|-----------------------------------------------------------------------|---------------------------------|-------------|----|----|----|------------------|------------------|------------------|------------------|------------------|-----|-----------------------|-------------|------|
|                                       | ID0                                                                   | hex                             | 15          | 14 | 13 | 12 | ...              | ...              | ...              | 1                | 0                |     |                       |             |      |
| DATA_ID                               |                                                                       |                                 | 0           | S  | G  | M  | x <sup>(2)</sup> | x <sup>(2)</sup> | x <sup>(2)</sup> | x <sup>(2)</sup> | x <sup>(2)</sup> |     |                       |             |      |
| Groups                                | 1/0                                                                   | 0x2000                          | 0           | 0  | 1  | 0  |                  |                  |                  |                  |                  | r/w | 8/4                   | 103         |      |
| SetGroup                              |                                                                       |                                 |             |    |    |    |                  |                  |                  |                  |                  |     |                       | 104         |      |
| StatusGroup                           |                                                                       |                                 |             |    |    |    |                  |                  |                  |                  |                  |     |                       | 106         |      |
| MonitorGroup                          |                                                                       |                                 |             |    |    |    |                  |                  |                  |                  |                  |     |                       | 108         |      |
| TripGroup                             |                                                                       |                                 |             |    |    |    |                  |                  |                  |                  |                  |     |                       | 111         |      |
| Temperatures                          | 1                                                                     | 0x2001                          | 0           | 0  | 1  | 0  |                  |                  | 0x001            |                  |                  | r   | 7                     | 113         |      |
| SupplyMeasurements                    | 1                                                                     | 0x2002                          | 0           | 0  | 1  | 0  |                  |                  | 0x002            |                  |                  | r   | 7                     | 113         |      |
| SupplyNominals                        | 1                                                                     | 0x2003                          | 0           | 0  | 1  | 0  |                  |                  | 0x003            |                  |                  |     |                       | 113         |      |
| GroupVoltageLimits                    | 1                                                                     | 0x2005                          | 0           | 0  | 1  | 0  |                  |                  | 0x005            |                  |                  | r   | 7                     | 113         |      |
| GroupCurrentLimits                    | 1                                                                     | 0x2006                          | 0           | 0  | 1  | 0  |                  |                  | 0x006            |                  |                  | r   | 7                     | 113         |      |
| VoltageSetAllChannels                 | 0                                                                     | 0x2100                          | 0           | 0  | 1  | 0  |                  |                  | 0x100            |                  |                  | w   | 6                     | 114         |      |
| Current-Trip/Set-AllChannels          | 0                                                                     | 0x2101                          | 0           | 0  | 1  | 0  |                  |                  | 0x101            |                  |                  | w   | 6                     | 114         |      |
| SetOnOffAllChannels                   | 0                                                                     | 0x2200                          | 0           | 0  | 1  | 0  |                  |                  | 0x200            |                  |                  | w   | 6                     | 115         |      |
| SetEmergencyAllChannels               | 0                                                                     | 0x2201                          | 0           | 0  | 1  | 0  |                  |                  | 0x201            |                  |                  | w   | 6                     | 116         |      |
| EventStatusVoltageLimitAllChannels    | 1/0                                                                   | 0x2202                          | 0           | 0  | 1  | 0  |                  |                  | 0x202            |                  |                  | r/w | 6                     | 117         |      |
| EventStatusCurrentLimitAllChannels    | 1/0                                                                   | 0x2203                          | 0           | 0  | 1  | 0  |                  |                  | 0x203            |                  |                  | r/w | 6                     | 118         |      |
| EventStatusCurrentTrip-AllChannels    | 1/0                                                                   | 0x2204                          | 0           | 0  | 1  | 0  |                  |                  | 0x204            |                  |                  | r/w | 6                     | 119         |      |
| EventStatusExternalInhibitAllChannels | 1/0                                                                   | 0x2205                          | 0           | 0  | 1  | 0  |                  |                  | 0x205            |                  |                  | r/w | 6                     | 117         |      |
| SetOnOffChannelsExtender              | 1/0                                                                   | 0x2280                          | 0           | 0  | 1  | 0  |                  |                  | 0x280            |                  |                  | r/w | 6                     | 121         |      |
| SetEmergencyChannels-Extender         | 1/0                                                                   | 0x2290                          | 0           | 0  | 1  | 0  |                  |                  | 0x290            |                  |                  | r/w | 6                     | 122         |      |
| Notes:                                |                                                                       |                                 |             |    |    |    |                  |                  |                  |                  |                  |     |                       |             |      |
| S                                     | DATA_ID type bit for a EDCP-frame of an access to single channel      |                                 |             |    |    |    |                  |                  |                  |                  |                  |     |                       |             |      |
| G                                     | DATA_ID type bit for a EDCP-frame of an access to a group of channels |                                 |             |    |    |    |                  |                  |                  |                  |                  |     |                       |             |      |
| M                                     | DATA_ID type bit for a EDCP-frame of an access to the whole module    |                                 |             |    |    |    |                  |                  |                  |                  |                  |     |                       |             |      |
| <sup>1)</sup>                         | Gn                                                                    | group access bits, (n=0 ... 11) |             |    |    |    |                  |                  |                  |                  |                  |     |                       |             |      |

Table 52: EDCP Group Accesses

### 3.4.4.5 Important DCP Module Access

| Access                                   | EXT_<br>INSTR | DATA_<br>DIR | Byte | DATA_ID<br>Bit |   |    |    |    |    |    |    | read /<br>write /<br>active | DATA-<br>Bytes | Page |
|------------------------------------------|---------------|--------------|------|----------------|---|----|----|----|----|----|----|-----------------------------|----------------|------|
|                                          | ID0           | ID1          |      | 7              | 6 | 5  | 4  | 3  | 2  | 1  | 0  |                             |                |      |
| Group access MODULE                      | 0             | 1/0          |      | 1              | 1 | M3 | M2 | M1 | M0 | R1 | R0 |                             |                |      |
| GeneralStatus                            | 0             | 1/0          | 0xc0 | 1              | 1 | 0  | 0  | 0  | 0  | 0  | 0  | a                           | 3              | 123  |
| LogOnOff Front-end at the superior layer | 0             | 1/0          | 0xD8 | 1              | 1 | 0  | 1  | 1  | 0  | 0  | 0  | a/w                         | 3              | 126  |
| Notes:                                   |               |              |      |                |   |    |    |    |    |    |    |                             |                |      |

Table 53: DCP Module Access

## 3.5 Description of data information per DATA\_ID in EDCP

### 3.5.1 EDCP Single Access

The single access describes the control of the channel properties. The range of the single access contains the accesses to the analog digital data items, to the status and the control words of the channels.

#### 3.5.1.1 Channel status (single/multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID       | CANNEL                                      | DATA_1        | DATA_0 |
|-------------------------|-----------------------|---------------|---------------------------------------------|---------------|--------|
| master single read-     | 1                     | 0x4000        | Mx                                          |               |        |
| master single MBR read- | 1                     | 0x6000        | Member                                      |               | Offset |
| HV board write access   | 0                     | 0x4000/0x6000 | Mx                                          | ChannelStatus |        |
| Notes:                  |                       |               |                                             |               |        |
| Mx                      | Channel               |               | 0 ... 255                                   |               |        |
| Member                  | Members               |               | 1 ... 16                                    |               |        |
| Offset                  | Channel member offset |               | 0, 16, 32 ... too access up to 255 channels |               |        |
| ChannelStatus           | DATA_0 to DATA_1      |               | UI2                                         |               |        |

Table 54: EDCP frame

#### 3.5.1.2 Channel status32 (single/multiple single read-write access)

| Access                  | DATA_DIR              | DATA_ID       | CHANNEL                                     | DATA_3          | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|---------------|---------------------------------------------|-----------------|--------|--------|--------|
| master single read-     | 1                     | 0x4080        | Mx                                          |                 |        |        |        |
| master single MBR read- | 1                     | 0x6080        | Member                                      |                 | Offset |        |        |
| HV board write access   | 0                     | 0x4080/0x6080 | Mx                                          | ChannelStatus32 |        |        |        |
| Notes:                  |                       |               |                                             |                 |        |        |        |
| Mx                      | Channel               |               | 0 ... 255                                   |                 |        |        |        |
| Member                  | Members               |               | 1 ... 16                                    |                 |        |        |        |
| Offset                  | Channel member offset |               | 0, 16, 32 ... too access up to 255 channels |                 |        |        |        |
| ChannelStatus32         | DATA_0 to DATA_3      |               | UI4                                         |                 |        |        |        |

Table 55: channel status32

| Bit31                   | Bit30                   | Bit29                | Bit28              | Bit27                     | Bit26                    | Bit25            | Bit24              |
|-------------------------|-------------------------|----------------------|--------------------|---------------------------|--------------------------|------------------|--------------------|
| Reserved                | Reserved                | Reserved             | Reserved           | Reserved                  | Reserved                 | Reserved         | Reserved           |
| Bit23                   | Bit22                   | Bit21                | Bit20              | Bit19                     | Bit18                    | Bit17            | Bit16              |
| isConstant Power        | isVoltage BoundLower    | isVoltage BoundUpper | isVoltage RampDown | isVoltage RampUp          | isCurrent RampDown       | isCurrent RampUp | isCurrent Ramping  |
| Bit15                   | Bit14                   | Bit13                | Bit12              | Bit11                     | Bit10                    | Bit09            | Bit08              |
| isVoltageLimit Exceeded | IsCurrentLimit Exceeded | isTrip Exceeded      | isExternal Inhibit | isVoltage Bounds Exceeded | isCurrent BoundsExceeded | isArcError       | isLowCurrentR ange |
| Bit07                   | Bit06                   | Bit05                | Bit04              | Bit03                     | Bit02                    | Bit01            | Bit00              |
| isConstant Voltage      | isConstant Current      | isEmergency          | isRamp             | isOn                      | inputError               | isArc            | Reserved           |

Table 56

The ChannelStatus register describes the actual status. Depending on the status of the module the bits will be set or reset.

The bit InputError will be set if the given parameter is not plausible or it exceeds the module parameters (e.g. if the command Vset=4000V is given to a module with NominalVoltage=3000V). The bit InputError is not be set if the given values are temporarily not possible (e.g. Vset=2800 at a module with NominalVoltage=3000V, but HardwareLimitVoltage=2500V). A certain signature which kind of input error it is does not exists.

| Bit                     | Description                                                                                                                                                                                                                                                                             |
|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| isVoltageLimitExceeded  | voltage limit set by Vmax is exceeded<br><br>isVoltageLimitExceeded=0 channel is ok<br>isVoltageLimitExceeded=1 the hardware voltage limit is exceeded                                                                                                                                  |
| isCurrentLimitExceeded  | current limit set by Imax is exceeded<br><br>isCurrentLimitExceeded=0 channel is ok<br>isCurrentLimitExceeded=1 the hardware current limit is exceeded (to detect a hardware voltage or current limit error flag the firmware has to evaluate the channel voltage and current at first) |
| isTripExceeded          | Trip is set when Voltage or Current limit or Iset has been exceeded (when KillEnable=1)<br><br>isTripExceeded=0 channel is ok<br>isTripExceeded=1 voltage output is shut off to 0V without ramp because the channel has been tripped.                                                   |
| isExternalInhibit       | External Inhibit<br><br>isExternalInhibit=0 channel is ok<br>isExternalInhibit=1 External Inhibit was scanned                                                                                                                                                                           |
| isVoltageBoundsExceeded | Voltage out of bounds<br><br>isVoltageBoundsExceeded=0 channel is ok<br>isVoltageBoundsExceeded=1 $ V_{meas} - V_{set}  > V_{bounds}$                                                                                                                                                   |
| isCurrentBoundsExceeded | Current out of bounds<br><br>isCurrentBoundsExceeded=0 channel is ok<br>isCurrentBoundsExceeded=1 $ I_{meas} - I_{set}  > I_{bounds}$ (to detect a voltage or current out of bound flag the firmware has to ramp the channel voltage Vset at first)                                     |

| Bit                        | Description                                                                                                                                                                                                                                                                                                                |
|----------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| isArcError                 | <p>maximum number of allowed arcs is exceeded, high voltage has been turned off</p> <p>isArcError=0      no arc error<br/>isArcError=1      maximum number of allowed arcs is exceeded</p>                                                                                                                                 |
| isLowCurrentRange          | <p>Low or small current range of the current measurement</p> <p>isLowCurrentRange=0      high or standard current range<br/>isLowCurrentRange=1      low current range of the current measurement</p>                                                                                                                      |
| isConstantVoltage          | <p>Voltage control active (evaluation is guaranteed when no ramp is running)</p> <p>isConstantVoltage=1      channel is in state of voltage control<br/>isConstantVoltage=0      channel is in state of current control</p>                                                                                                |
| isContstantCurrent         | <p>Current control active (evaluation is guaranteed when no ramp is running)</p>                                                                                                                                                                                                                                           |
| isEmergencyOff             | <p>Emergency off without ramp</p> <p>IsEmergencyOff=1      channel is in state of emergency off, VO has been shut off to 0V without ramp</p>                                                                                                                                                                               |
| isOn                       | <p>On</p> <p>isOn=0      channel is off<br/>isOn=1      channel voltage follows the Vset value</p>                                                                                                                                                                                                                         |
| isRamping                  | <p>Ramp is running</p> <p>isRamping=0      no voltage is in change<br/>isRamping=1      voltage is in change with the stored ramp speed value</p>                                                                                                                                                                          |
| inputError                 | <p>Input error</p> <p>inputError=0      no input-error<br/>inputError=1      incorrect message to control the channel</p>                                                                                                                                                                                                  |
| isArc or IsRegulationError | <p>at least one electrical arc is active or<br/>faster error detection of the channel hardware is not in regulation (updated by firmware every 5ms)</p> <p>isArc=0      no arc active / normal error evaluation<br/>isArc=1      at least one electrical arc is active / fast detection of a regulation error (OPTION)</p> |
| isPositive                 | reserved                                                                                                                                                                                                                                                                                                                   |

Table 57

### 3.5.1.3 Channel control: (single write- and single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID                                    | CHN    | DATA_1         |
|-------------------------|-----------------------|--------------------------------------------|--------|----------------|
| master write access     | 0                     | 0x4001                                     | Mx     |                |
| master read-            | 1                     | 0x4001                                     | Mx     | ChannelControl |
| master single MBR read- | 1                     | 0x6001                                     | Member | Offset         |
| HV board write access   | 0                     | 0x4001/0x6001                              | Mx     | ChannelControl |
| Notes:                  |                       |                                            |        |                |
| Mx                      | Channel               | 0 ... 255                                  |        |                |
| Member                  | Members               | 1 ... 16                                   |        |                |
| Offset                  | Channel member offset | 0, 16, 32 ... to access up to 255 channels |        |                |

Table 58: channel control

### 3.5.1.4 Channel control32: (single write- and single/ multiple single read-write access)

| Access                  | DATA_DIR              | DATA_ID                                    | CHANNEL | DATA_3           | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|--------------------------------------------|---------|------------------|--------|--------|--------|
| master single read-     | 1                     | 0x4081                                     | Mx      |                  |        |        |        |
| master single MBR read- | 1                     | 0x6081                                     | Member  |                  | Offset |        |        |
| HV board write access   | 0                     | 0x4081/0x6081                              | Mx      | ChannelControl32 |        |        |        |
| Notes:                  |                       |                                            |         |                  |        |        |        |
| Mx                      | Channel               | 0 ... 255                                  |         |                  |        |        |        |
| Member                  | Members               | 1 ... 16                                   |         |                  |        |        |        |
| Offset                  | Channel member offset | 0, 16, 32 ... to access up to 255 channels |         |                  |        |        |        |
| ChannelControl32        | DATA_0 to DATA_3      | UI4                                        |         |                  |        |        |        |

Table 59: channel control32

ChannelControl DATA\_0 to DATA\_3 UI4

| Bit31    | Bit30    | Bit29    | Bit28    | Bit27    | Bit26    | Bit25    | Bit24    |
|----------|----------|----------|----------|----------|----------|----------|----------|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Bit23    | Bit22    | Bit21    | Bit20    | Bit19    | Bit18    | Bit17    | Bit16    |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Bit15    | Bit14    | Bit13    | Bit12    | Bit11    | Bit10    | Bit09    | Bit08    |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Bit07    | Bit06    | Bit05    | Bit04    | Bit03    | Bit02    | Bit01    | Bit00    |
| Reserved | Reserved | setEMCY  | Reserved | setON    | Reserved | Reserved | Reserved |

Table 60: channel control data

The signals SetOn and SetEmergencyOff control are basic functions of the channel. The signal SetOn is switching ON the HV of the channel and is a precondition for giving voltage to the output. As far as a VoltageSet has been set and no event has occurred and is not registered yet (in minimum, bit 5 and bit 10 to 15 of the register Channel Event Status must be 0), a start of a HV ramp will be synchronized (a ramp is a software controlled, time proportionally increase / decrease of the output voltage ).

A SetEmergencyOff switch the channel in state isEmergencyOff and a new SetOn is only possible after SetEmergencyOff is reset to zero.

| Bit     | Name            | Description                                                                                                              |
|---------|-----------------|--------------------------------------------------------------------------------------------------------------------------|
| setEMCY | SetEmergencyOff | Set "Emergency Off"<br><br>SetEMCY=0 channel emergency cut-off works<br>setEMCY=1 cut-off VO shut off to 0V without ramp |
| setON   | SetOn           | Set On<br><br>setOn=0 switch the channel to OFF<br>setOn=1 switch the channel to ON                                      |
| res     | Reserved        | Reserved                                                                                                                 |

Table 61

### 3.5.1.5 Channel event status (single write- and single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID       | CHN                                        | DATA_1             | DATA_0 |
|-------------------------|-----------------------|---------------|--------------------------------------------|--------------------|--------|
| master write access     | 0                     | 0x4002        | Mx                                         |                    |        |
| master read-            | 1                     | 0x4002        | Mx                                         | ChannelEventStatus |        |
| master single MBR read- | 1                     | 0x6002        | Member                                     |                    |        |
|                         |                       |               |                                            |                    | Offset |
| HV board write access   | 0                     | 0x4002/0x6002 | Mx                                         | ChannelEventStatus |        |
| Notes:                  |                       |               |                                            |                    |        |
| Mx                      | Channel               |               | 0 ... 255                                  |                    |        |
| Member                  | Members               |               | 1 ... 16                                   |                    |        |
| Offset                  | Channel member offset |               | 0, 16, 32 ... to access up to 255 channels |                    |        |

Table 62: EDCP frame

### 3.5.1.6 Channel event status32 (single write- and single/ multiple single read-write access)

| Access                  | DATA_DIR              | DATA_ID       | CHANNEL                                    | DATA_3               | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|---------------|--------------------------------------------|----------------------|--------|--------|--------|
| master single read-     | 1                     | 0x4082        | Mx                                         |                      |        |        |        |
| master single MBR read- | 1                     | 0x6082        | Member                                     |                      | Offset |        |        |
| HV board write access   | 0                     | 0x4082/0x6082 | Mx                                         | ChannelEventStatus32 |        |        |        |
| Notes:                  |                       |               |                                            |                      |        |        |        |
| Mx                      | Channel               |               | 0 ... 255                                  |                      |        |        |        |
| Member                  | Members               |               | 1 ... 16                                   |                      |        |        |        |
| Offset                  | Channel member offset |               | 0, 16, 32 ... to access up to 255 channels |                      |        |        |        |
| ChannelEventStatus32    | DATA_0 to DATA_3      |               | UI4                                        |                      |        |        |        |

Table 63: channel event status32

ChannelEventStatus      DATA\_0 to DATA\_3      UI4

| Bit31                       | Bit30                       | Bit29                  | Bit28                  | Bit27                       | Bit26                        | Bit25               | Bit24                  |
|-----------------------------|-----------------------------|------------------------|------------------------|-----------------------------|------------------------------|---------------------|------------------------|
| Reserved                    | Reserved                    | Reserved               | Reserved               | Reserved                    | Reserved                     | Reserved            | EventMax Power         |
| Bit23                       | Bit22                       | Bit21                  | Bit20                  | Bit19                       | Bit18                        | Bit17               | Bit16                  |
| EventCon-stantPower         | EventVoltage BoundLower     | EventVoltageBoundUpper | EventVoltage RampDown  | EventVoltage RampUp         | EventCurrent RampDown        | EventCurrent RampUp | EventEndOf CurrentRamp |
| Bit15                       | Bit14                       | Bit13                  | Bit12                  | Bit11                       | Bit10                        | Bit09               | Bit08                  |
| EventVoltage Limit Exceeded | EventCurrent Limit Exceeded | EventTrip              | Event External Inhibit | EventVoltageBounds Exceeded | EventCurrent Bounds Exceeded | EventArc Error      | Reserved               |
| Bit07                       | Bit06                       | Bit05                  | Bit04                  | Bit03                       | Bit02                        | Bit01               | Bit00                  |
| EventCon-stantVoltage       | EventCon-stantCurrent       | Event Emergency        | EventEndOfVoltageRamp  | EOn2Off                     | EventInput Error             | EventArc            | Reserved               |

Table 64: channel event status data

| Bit                       | Blocking | Description                                                                                                                                                                     |
|---------------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EventMaxPower             |          |                                                                                                                                                                                 |
| EventConstantPower        |          | Constant Power has been or is active                                                                                                                                            |
| EventVoltageBoundLower    |          | The measured voltage has been or is lower than the programmed lower bound                                                                                                       |
| EventVoltageBoundUpper    |          | The measured voltage has been or is higher than the programmed upper bound                                                                                                      |
| EventVoltageRampDown      |          | Voltage ramp down to a lower absolute value has been started                                                                                                                    |
| EventVoltageRampUp        |          | Voltage ramp up to a higher absolute value has been started                                                                                                                     |
| EventCurrentRampDown      |          | Current ramp down has been started                                                                                                                                              |
| EventCurrentRampUp        |          | Current ramp up has been started                                                                                                                                                |
| EventEndOfCurrentRamp     |          | A running current ramp has reached its destination                                                                                                                              |
| EventVoltageLimitExceeded | Yes      | Voltage limit Vlim has been or is exceeded                                                                                                                                      |
| EventCurrentLimitExceeded | Yes      | Current limit Ilim has been or is exceeded                                                                                                                                      |
| EventTrip                 | Yes      | Event: Trip is set when Voltage or Current limit or Iset has been exceeded (when KillEnable=1 or Delayed Trip is configured)                                                    |
| EventExternalInhibit      | Yes      | External Inhibit has been or is active                                                                                                                                          |
| EventVoltageBounds        |          | Measured voltage has been or is out of bounds                                                                                                                                   |
| EventCurrentBounds        |          | Measured current has been or is out of bounds                                                                                                                                   |
| EventArcError             |          | An Arc Error event has occurred                                                                                                                                                 |
| EventConstantVoltage      |          | Constant Voltage has been or is active                                                                                                                                          |
| EventConstantCurrent      |          | Constant Current has been or is active                                                                                                                                          |
| EventEmergencyOff         | Yes      | Channel was shut down with emergency off                                                                                                                                        |
| EventEndOfRamp            |          | A running voltage ramp has reached its destinationThe channel was switched off due to a blocking event (Voltage/Current Limit, Current Trip, External Inhibit or Emergency Off) |
| EventOnToOff              |          | The channel was switched off due to a blocking event (Voltage/Current Limit, Current Trip, External Inhibit or Emergency Off)                                                   |
| EventInputError           |          | An Input Error has occurred                                                                                                                                                     |
| EventArc                  |          | Arc or Regulation Error has been or is active                                                                                                                                   |

Table 65

An event bit is permanently set if the status bit is 1 or is changing to 1. Different to the status bit an event bit isn't automatically reset. A reset has to be done by the user by writing an 1 to this event bit.

### 3.5.1.7 Channel event mask (single write- and single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID       | CHANNEL                                    | DATA_1           | DATA_0 |
|-------------------------|-----------------------|---------------|--------------------------------------------|------------------|--------|
| master write access     | 0                     | 0x4003        | Mx                                         |                  |        |
| master read-            | 1                     | 0x4003        | Mx                                         | ChannelEventMask |        |
| master single MBR read- | 1                     | 0x6003        | MemberOffset                               |                  |        |
| HV board write access   | 0                     | 0x4003/0x6003 | Mx                                         | ChannelEventMask |        |
| Notes:                  |                       |               |                                            |                  |        |
| Mx                      | Channel               |               | 0 ... 255                                  |                  |        |
| Member                  | Members               |               | 1 ... 16                                   |                  |        |
| Offset                  | Channel member offset |               | 0, 16, 32 ... to access up to 255 channels |                  |        |
| ChannelEventMask        | DATA_0 to DATA_1      |               | UI2                                        |                  |        |

Table 66: channel event mask

### 3.5.1.8 Channel event mask32 (single write- and single/ multiple single read-write access)

| Access                  | DATA_DIR              | DATA_ID       | CHANNEL                                    | DATA_3               | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|---------------|--------------------------------------------|----------------------|--------|--------|--------|
| master single read-     | 1                     | 0x4083        | Mx                                         |                      |        |        |        |
| master single MBR read- | 1                     | 0x6083        | Member                                     |                      | Offset |        |        |
| HV board write access   | 0                     | 0x4083/0x6083 | Mx                                         | ChannelEventStatus32 |        |        |        |
| Notes:                  |                       |               |                                            |                      |        |        |        |
| Mx                      | Channel               |               | 0 ... 255                                  |                      |        |        |        |
| Member                  | Members               |               | 1 ... 16                                   |                      |        |        |        |
| Offset                  | Channel member offset |               | 0, 16, 32 ... to access up to 255 channels |                      |        |        |        |
| ChannelEventMask32      | DATA_0 to DATA_3      |               | UI4                                        |                      |        |        |        |

Table 67: channel event mask32

ChannelEventMask DATA\_0 to DATA\_3

UI4

| Bit31                            | Bit30                              | Bit29                              | Bit28                             | Bit27                          | Bit26                            | Bit25                          | Bit24                             |
|----------------------------------|------------------------------------|------------------------------------|-----------------------------------|--------------------------------|----------------------------------|--------------------------------|-----------------------------------|
| Reserved                         | Reserved                           | Reserved                           | Reserved                          | Reserved                       | Reserved                         | Reserved                       | Reserved                          |
| Bit23                            | Bit22                              | Bit21                              | Bit20                             | Bit19                          | Bit18                            | Bit17                          | Bit16                             |
| Reserved                         | MaskEvent<br>Voltage<br>BoundLower | MaskEvent<br>Voltage<br>BoundUpper | MaskEvent<br>Voltage<br>RampDown  | MaskEvent<br>Voltage<br>RampUp | MaskEvent<br>Current<br>RampDown | MaskEvent<br>Current<br>RampUp | MaskEvent<br>EndOf<br>CurrentRamp |
| Bit15                            | Bit14                              | Bit13                              | Bit12                             | Bit11                          | Bit10                            | Bit09                          | Bit08                             |
| MaskEvent<br>VoltageLimit        | MaskEvent<br>CurrentLimit          | MaskEvent<br>Trip                  | MaskEvent<br>External<br>Inhibit  | MaskEvent<br>Voltage<br>Bounds | MaskEvent<br>Current<br>Bounds   | MaskEvent<br>ArcError          | Reserved                          |
| Bit07                            | Bit06                              | Bit05                              | Bit04                             | Bit03                          | Bit02                            | Bit01                          | Bit00                             |
| MaskEvent<br>Constant<br>Voltage | MaskEvent<br>Constant<br>Current   | Reserved                           | MaskEvent<br>EndOf<br>VoltageRamp | MaskEvent On<br>To Off         | MaskEvent<br>Input Error         | MaskEvent<br>ARC               | Reserved                          |

Table 68: channel event mask data

The function of the ChannelEventMask register is described in 3.5.5.1 Channel events

| Bit                                      | Description                                                                                 |
|------------------------------------------|---------------------------------------------------------------------------------------------|
| MaskEventMaxPower                        | Mask the Event Max Power                                                                    |
| MaskEventConstantPower                   | Mask the Event Constant Power                                                               |
| MaskEventVoltageBoundLower               | Mask the Event Voltage Bound Exceeded Lower                                                 |
| MaskEventVoltageBoundUpper               | Mask the Event Voltage Bound Exceeded Upper                                                 |
| MaskEventVoltageRampDown                 | Mask the Event Voltage Ramp Down                                                            |
| MaskEventVoltageRampUp                   | Mask the Event Voltage Ramp Up                                                              |
| MaskEventCurrentRampDown                 | Mask the Event Current Ramp Down                                                            |
| MaskEventCurrentRampUp                   | Mask the Event Current Ramp Up                                                              |
| MaskEventEndOfCurrentRamp                | Mask the Event End Of Current Ramp                                                          |
| MaskEventVoltageLimit                    | Mask the Event Hardware- voltage limit has been exceeded                                    |
| MaskEventCurrentLimit                    | Mask the Event Hardware- current limit has been exceeded                                    |
| MaskEventTrip                            | Mask the Event Voltage limit or Current limit or Iset has been exceeded (when KillEnable=1) |
| MaskEventExtInhibit                      | Mask the Event External Inhibit                                                             |
| MaskEventVoltageBounds                   | Mask the Event Voltage out of bounds                                                        |
| MaskEventCurrentBounds                   | Mask the Event Current out of bounds                                                        |
| MaskEventArcError                        | Mask the Event Arc error                                                                    |
| MaskEventConstantVoltage                 | Mask the Event Constant Voltage                                                             |
| MaskEventConstantCurrent                 | Mask the Event Constant Current                                                             |
| MaskEventEndOfRamp                       | Mask the Event End Of Voltage Ramp                                                          |
| MaskEventOnToOff                         | Mask the Event change from state on to off                                                  |
| MaskEventInputError                      | Mask the Event Input Error                                                                  |
| MaskEventArc<br>MaskEventRegulationError | Mask the Event Arc active<br>Mask the Regulation Error (Option - fast error evaluation)     |

Table 69

#### CAUTION!



CAUTION!

Module in mode KILL disable:  
If a bit of the ChannelEventStatus register is set to "1" and the corresponding bit in the ChannelEventMask register is "0", it is not necessary to clear the ChannelEventStatus bit to switch on HV again.

If a bit of the ChannelEventMask register is set to "1" and if the corresponding bit in the ChannelEventStatus is set to "1" by the module firmware then a reset of the corresponding ChannelEventStatus bits is necessary before a switch on the HV of this channel is possible again.

Module in mode KILL enable: A reset of the ChannelEventStatus bits is necessary before switch on the HV of this channel again.

### 3.5.1.9 Delayed trip time

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID         | CHN                                        | DATA_1 | DATA_0 |
|-------------------------|-----------------------|-----------------|--------------------------------------------|--------|--------|
| master single read-     | 1                     | 0x4005          | Mx                                         |        |        |
| master single MBR read- | 1                     | 0x4005          | Member                                     |        | Offset |
| HV board write access   | 0                     | 0x4005 / 0x6003 | Mx                                         |        |        |
| Notes:                  |                       |                 |                                            |        |        |
| Mx                      | Channel               |                 | 0 ... 255                                  |        |        |
| Member                  | Members               |                 | 1 ... 16                                   |        |        |
| Offset                  | Channel member offset |                 | 0, 16, 32 ... to access up to 255 channels |        |        |
| Timeout-time            | DATA_0 to DATA_1[ms]  |                 | UI2 (Range 1 to 4095 ms)                   |        |        |

Table 70: trip time

Time in milliseconds until delayed trip action becomes active and channel is in current control state. Note special functionality for modules with a second low current range – see manual “Delayed trip EHS.pdf”, see 4 Appendix.

### 3.5.1.10 Delayed trip action (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID | CHN                                        | DATA_0 | DATA_1 | DATA_2 |
|-------------------------|-----------------------|---------|--------------------------------------------|--------|--------|--------|
| master write access     | 0                     | 0x4006  | Mx                                         | Action |        |        |
| master read-            | 1                     | 0x4006  | Mx                                         |        |        |        |
| master single MBR read- | 1                     | 0x6006  | Member                                     |        | Offset | Action |
| HV board write access   | 0                     | 0x4006  | Mx                                         | Action |        |        |
| Notes:                  |                       |         |                                            |        |        |        |
| Mx                      | Channel               |         | 0 ... 255                                  |        |        |        |
| Member                  | Members               |         | 1 ... 16                                   |        |        |        |
| Offset                  | Channel member offset |         | 0, 16, 32 ... to access up to 255 channels |        |        |        |

Table 71: trip action

| Action | Action if a trip event will be initiated           |
|--------|----------------------------------------------------|
| 0      | no action                                          |
| 1      | ramp down high voltage of the channel              |
| 2      | shut down high voltage of the channel without ramp |
| 3      | shut down the whole module without ramp            |
| 4      | switch off the delayed trip function               |

Table 72

### 3.5.1.11 External channel inhibit

EDCP frame:

| Access                   | DATA_DIR              | DATA_ID         | CHN                                        | DATA_0 | DATA_1 | DATA_2 |
|--------------------------|-----------------------|-----------------|--------------------------------------------|--------|--------|--------|
| master write access      | 0                     | 0x4007          | Mx                                         | Action |        |        |
| master read-             | 1                     | 0x4007          | Mx                                         |        |        |        |
| master single MBR write- | 1                     | 0x6007          | Member                                     |        | Offset | Action |
| HV board write access    | 0                     | 0x4007 / 0x6007 | Mx                                         | Action |        |        |
| Notes:                   |                       |                 |                                            |        |        |        |
| Mx                       | Channel               |                 | 0 ... 255                                  |        |        |        |
| Member                   | Members               |                 | 1 ... 16                                   |        |        |        |
| Offset                   | Channel member offset |                 | 0, 16, 32 ... to access up to 255 channels |        |        |        |

Table 73: external channel inhibit

| Action | Action if an inhibit signal will be triggered      |
|--------|----------------------------------------------------|
| 0      | no action                                          |
| 1      | ramp down high voltage of the channel              |
| 2      | shut down high voltage of the channel without ramp |
| 3      | shut down the whole module without ramp            |
| 4      | switch off the external inhibit function           |

Table 74

### 3.5.1.12 VoltageRampPriority (single write- and single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID         | CHN                                        | DATA_1 | DATA_0 |
|-------------------------|-----------------------|-----------------|--------------------------------------------|--------|--------|
| master single read-     | 1                     | 0x4010          | Mx                                         |        |        |
| master single MBR read- | 1                     | 0x4010          | Member                                     |        | Offset |
| HV board write access   | 0                     | 0x4010 / 0x6010 | Mx                                         |        |        |
| Notes:                  |                       |                 |                                            |        |        |
| Mx                      | Channel               |                 | 0 ... 255                                  |        |        |
| Member                  | Members               |                 | 1 ... 16                                   |        |        |
| Offset                  | Channel member offset |                 | 0, 16, 32 ... to access up to 255 channels |        |        |
| VoltageRampPriority     | DATA_0 to DATA_1      | UI2             | (Range 0 to channel number)                |        |        |

Table 75: voltage ramp priority

Time in milliseconds until delayed trip action becomes active and channel is in current control state. Note special

### 3.5.1.13 Set voltage (single write- and single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID       | CHN                                        | DATA_3     | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|---------------|--------------------------------------------|------------|--------|--------|--------|
| master write access     | 0                     | 0x4100        | Mx                                         | VoltageSet |        |        |        |
| master read -           | 1                     | 0x4100        | Mx                                         |            |        |        |        |
| master single MBR read- | 1                     | 0x6100        | Member                                     |            | Offset |        |        |
| HV board write access   | 0                     | 0x4100/0x6100 | Mx                                         | VoltageSet |        |        |        |
| Notes:                  |                       |               |                                            |            |        |        |        |
| Mx                      | Channel               |               | 0 ... 255                                  |            |        |        |        |
| Member                  | Members               |               | 1 ... 16                                   |            |        |        |        |
| Offset                  | Channel member offset |               | 0, 16, 32 ... to access up to 255 channels |            |        |        |        |
| VoltageSet              | DATA_0 to DATA_3 [V]  |               | R4                                         |            |        |        |        |

Table 76: set voltage

The VoltageSet value is the preset for voltage generation. Allowed values are between 0 and the actual hardware limit value. If written values are between the hardware limit and the nominal value, then the module reduces these values to the value of the actual hardware limit. If written values are higher than the nominal data or lower than 0 an input error is indicated by setting the bit InputError.

If the channel is switched 'ON' then the voltage will be ramped to the set value after the receipt of this access. Otherwise the set value will just be stored and only used for ramping to the set voltage after the channel will be switched 'ON'.

### 3.5.1.14 Set current / trip (single write- and single/ multiple single read-write access)

EDCP frame:

| Access                   | DATA_DIR              | DATA_ID       | CHN                                        | DATA_3                   | DATA_2 | DATA_1 | DATA_0 |
|--------------------------|-----------------------|---------------|--------------------------------------------|--------------------------|--------|--------|--------|
| master write access      | 0                     | 0x4101        | Mx                                         | CurrentSet (CurrentTrip) |        |        |        |
| master read -            | 1                     | 0x4101        | Mx                                         |                          |        |        |        |
| master single MBR read-  | 1                     | 0x6101        | Member                                     |                          | Offset |        |        |
| HV board write access    | 0                     | 0x4101/0x6101 | Mx                                         | CurrentSet (CurrentTrip) |        |        |        |
| Notes:                   |                       |               |                                            |                          |        |        |        |
| Mx                       | Channel               |               | 0 ... 255                                  |                          |        |        |        |
| Member                   | Members               |               | 1 ... 16                                   |                          |        |        |        |
| Offset                   | Channel member offset |               | 0, 16, 32 ... to access up to 255 channels |                          |        |        |        |
| CurrentSet (CurrentTrip) | DATA_0 to DATA_3 [A]  |               | R4                                         |                          |        |        |        |

Table 77: set current

Allowed values are between 0 and the actual hardware limit value. If written values are between the hardware limit and the nominal value, then the module reduces these values to the value of the actual hardware limit. If written values are higher than the nominal data or lower than 0 an input error is indicated by setting the bit InputError.

The mode of action of this item depends on the setting of the signal Kill Enable (KILEna) in the ModuleControl register (see chapter 3.5.2.3 ModuleControl (module write- / read-write access)). If Kill Enable is 0, the value is interpreted as CurrentSet. If Kill Enable is 1, the value is CurrentTrip.

### CurrentSet:

The CurrentSet value is the preset for current regulation. If the output current reaches or exceeds the Current Set value, the channel goes into Current Regulation mode. In this mode the output current is regulated at the CurrentSet value, but the output voltage is going to a value between 0V and Vset, depending of the external load.

When Current Control mode is active the bit isConstantCurrent of the ChannelStatus register and the bit EventConstantCurrent of the ChannelEventStatus are set, the bit isConstantVoltage of the ChannelStatus is reset.

### CurrentTrip:

In Current Trip mode this value will be used as software current trip. If exceeding this value a current trip event will be registered. The green LED on front panel will be switched off.

The bits isTrip in the ChannelStatus and ETRP in ChannelEventStatus are set, the bit isNoSumError in the ModuleStatus is reset.

### 3.5.1.15 Voltage measurement (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID       | CHN                                        | DATA_3         | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|---------------|--------------------------------------------|----------------|--------|--------|--------|
| master read -           | 1                     | 0x4102        | Mx                                         |                |        |        |        |
| master single MBR read- | 1                     | 0x6102        | Member                                     |                | Offset |        |        |
| HV board write access   | 0                     | 0x4102/0x6102 | Mx                                         | VoltageMeasure |        |        |        |
| Notes:                  |                       |               |                                            |                |        |        |        |
| Mx                      | Channel               |               | 0 ... 255                                  |                |        |        |        |
| Member                  | Members               |               | 1 ... 16                                   |                |        |        |        |
| Offset                  | Channel member offset |               | 0, 16, 32 ... to access up to 255 channels |                |        |        |        |
| VoltageMeasure          | DATA_0 to DATA_3 [V]  |               | R4                                         |                |        |        |        |

Table 78: voltage measurement

### 3.5.1.16 Current measurement (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID       | CHN                                        | DATA_3         | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|---------------|--------------------------------------------|----------------|--------|--------|--------|
| master read -           | 1                     | 0x4103        | Mx                                         |                |        |        |        |
| master single MBR read- | 1                     | 0x6103        | Member                                     |                | Offset |        |        |
| HV board write access   | 0                     | 0x4103/0x6103 | Mx                                         | CurrentMeasure |        |        |        |
| Notes:                  |                       |               |                                            |                |        |        |        |
| Mx                      | Channel               |               | 0 ... 255                                  |                |        |        |        |
| Member                  | Members               |               | 1 ... 16                                   |                |        |        |        |
| Offset                  | Channel member offset |               | 0, 16, 32 ... to access up to 255 channels |                |        |        |        |
| CurrentMeasure          | DATA_0 to DATA_3 [A]  |               | R4                                         |                |        |        |        |

Table 79: current measurement

### 3.5.1.17 Voltage bounds (single write- / single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID         | CHN                                        | DATA_3        | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|-----------------|--------------------------------------------|---------------|--------|--------|--------|
| master write access     | 0                     | 0x4104          | MX                                         | VoltageBounds |        |        |        |
| master read -           | 1                     | 0x4104          | MX                                         |               |        |        |        |
| master single MBR read- | 1                     | 0x6104          | Member                                     |               | Offset |        |        |
| HV board write access   | 0                     | 0x4104 / 0x6104 | MX                                         | VoltageBounds |        |        |        |
| Notes:                  |                       |                 |                                            |               |        |        |        |
| Mx                      | Channel               |                 | 0 ... 255                                  |               |        |        |        |
| Member                  | Members               |                 | 1 ... 16                                   |               |        |        |        |
| Offset                  | Channel member offset |                 | 0, 16, 32 ... to access up to 255 channels |               |        |        |        |
| VoltageBounds           | DATA_0 to DATA_3 [V]  |                 | R4 (0 to VoltageNominal)                   |               |        |        |        |

Table 80: voltage bounds

### 3.5.1.18 Current bounds (single write- / single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID         | CHN                                        | DATA_3        | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|-----------------|--------------------------------------------|---------------|--------|--------|--------|
| master write access     | 0                     | 0x4105          | MX                                         | CurrentBounds |        |        |        |
| master read -           | 1                     | 0x4105          | MX                                         |               |        |        |        |
| master single MBR read- | 1                     | 0x6105          | Member                                     |               | Offset |        |        |
| HV board write access   | 0                     | 0x4105 / 0x6105 | MX                                         | CurrentBounds |        |        |        |
| Notes:                  |                       |                 |                                            |               |        |        |        |
| Mx                      | Channel               |                 | 0 ... 255                                  |               |        |        |        |
| Member                  | Members               |                 | 1 ... 16                                   |               |        |        |        |
| Offset                  | Channel member offset |                 | 0, 16, 32 ... to access up to 255 channels |               |        |        |        |
| CurrentBounds           | DATA_0 to DATA_3 [A]  |                 | R4 (0 to CurrentNominal)                   |               |        |        |        |

Table 81: current bounds

### 3.5.1.19 Nominal voltage (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID         | CHN                                        | DATA_3         | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|-----------------|--------------------------------------------|----------------|--------|--------|--------|
| master read -           | 1                     | 0x4106          | MX                                         |                |        |        |        |
| master single MBR read- | 1                     | 0x6106          | Member                                     |                | Offset |        |        |
| HV board write access   | 0                     | 0x4106 / 0x6106 | MX                                         | VoltageNominal |        |        |        |
| Notes:                  |                       |                 |                                            |                |        |        |        |
| Mx                      | Channel               |                 | 0 ... 255                                  |                |        |        |        |
| Member                  | Members               |                 | 1 ... 16                                   |                |        |        |        |
| Offset                  | Channel member offset |                 | 0, 16, 32 ... to access up to 255 channels |                |        |        |        |
| VoltageNominal          | DATA_0 to DATA_3 [V]  |                 | R4                                         |                |        |        |        |

Table 82

### 3.5.1.20 Nominal current (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID         | CHN                                        | DATA_3         | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|-----------------|--------------------------------------------|----------------|--------|--------|--------|
| master read -           | 1                     | 0x4107          | MX                                         |                |        |        |        |
| master single MBR read- | 1                     | 0x6107          | Member                                     |                | Offset |        |        |
| HV board write access   | 0                     | 0x4107 / 0x6107 | MX                                         | CurrentNominal |        |        |        |
| Notes:                  |                       |                 |                                            |                |        |        |        |
| Mx                      | Channel               |                 | 0 ... 255                                  |                |        |        |        |
| Member                  | Members               |                 | 1 ... 16                                   |                |        |        |        |
| Offset                  | Channel member offset |                 | 0, 16, 32 ... to access up to 255 channels |                |        |        |        |
| CurrentNominal          | DATA_0 to DATA_3 [A]  |                 | R4                                         |                |        |        |        |

Table 83: nominal current

### 3.5.1.21 Nominal power (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID         | CHN                                        | DATA_3       | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|-----------------|--------------------------------------------|--------------|--------|--------|--------|
| master read -           | 1                     | 0x4108          | MX                                         |              |        |        |        |
| master single MBR read- | 1                     | 0x6108          | Member                                     |              | Offset |        |        |
| HV board write access   | 0                     | 0x4108 / 0x6108 | MX                                         | PowerNominal |        |        |        |
| Notes:                  |                       |                 |                                            |              |        |        |        |
| Mx                      | Channel               |                 | 0 ... 255                                  |              |        |        |        |
| Member                  | Members               |                 | 1 ... 16                                   |              |        |        |        |
| Offset                  | Channel member offset |                 | 0, 16, 32 ... to access up to 255 channels |              |        |        |        |
| PowerNominal            | DATA_0 to DATA_3 [W]  |                 | R4                                         |              |        |        |        |

Table 84: nominal power

### 3.5.1.22 Current measurement range<sup>2</sup> (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR                      | DATA_ID         | CHN                                        | DATA_4         | DATA_3 | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-------------------------------|-----------------|--------------------------------------------|----------------|--------|--------|--------|--------|
| master read -           | 1                             | 0x4109          | MX                                         |                |        |        |        |        |
| master single MBR read- | 1                             | 0x6109          | Member                                     |                | Offset |        |        |        |
| HV board write access   | 0                             | 0x4109 / 0x6109 | MX                                         | CurrentMeasure |        |        |        | Range  |
| Notes:                  |                               |                 |                                            |                |        |        |        |        |
| Mx                      | Channel                       |                 | 0 ... 255                                  |                |        |        |        |        |
| Member                  | Members                       |                 | 1 ... 16                                   |                |        |        |        |        |
| Offset                  | Channel member offset         |                 | 0, 16, 32 ... to access up to 255 channels |                |        |        |        |        |
| CurrentMeasure          | DATA_1 to DATA_4 [A]          |                 | R4                                         |                |        |        |        |        |
| Range                   | DATA_0=0 – high range (≥20μA) |                 | UI1                                        |                |        |        |        |        |
|                         | DATA_0=1 – low range (<20μA)  |                 |                                            |                |        |        |        |        |

Table 85: current measurement range

**INFORMATION**



The information channel status bit is `LowCurrentRange` can be used also.

**INFORMATION**

### 3.5.1.23 VoltageBottom (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR                                  | DATA_ID       | CHN                                        | DATA_3        | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-------------------------------------------|---------------|--------------------------------------------|---------------|--------|--------|--------|
| master write access     | 0                                         | 0x410A        | Mx                                         | VoltageBottom |        |        |        |
| master read -           | 1                                         | 0x410A        | Mx                                         |               |        |        |        |
| master single MBR read- | 1                                         | 0x610A        | Member                                     |               | Offset |        |        |
| HV board write access   | 0                                         | 0x410A/0x610A | Mx                                         | VoltageBottom |        |        |        |
| Notes:                  |                                           |               |                                            |               |        |        |        |
| Mx                      | Channel                                   |               | 0 ... 255                                  |               |        |        |        |
| Member                  | Members                                   |               | 1 ... 16                                   |               |        |        |        |
| Offset                  | Channel member offset                     |               | 0, 16, 32 ... to access up to 255 channels |               |        |        |        |
| VoltageBottom           | DATA_0 to DATA_3 [% of V <sub>set</sub> ] |               | R4                                         |               |        |        |        |

Table 86: voltage bottom

2 - for devices E08F2, E08F7, E08C2, N06C2 and N04C2 only

### 3.5.1.24 VCT Coefficient<sup>3</sup> (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR               | DATA_ID       | CHN    | DATA_3                                     | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|------------------------|---------------|--------|--------------------------------------------|--------|--------|--------|
| master write access     | 0                      | 0x4120        | Mx     | VctCoefficient                             |        |        |        |
| master read -           | 1                      | 0x4120        | Mx     |                                            |        |        |        |
| master single MBR read- | 1                      | 0x6120        | Member |                                            | Offset |        |        |
| HV board write access   | 0                      | 0x4120/0x6120 | Mx     | VctCoefficient                             |        |        |        |
| Notes:                  |                        |               |        |                                            |        |        |        |
| Mx                      | Channel                |               |        | 0 ... 255                                  |        |        |        |
| Member                  | Members                |               |        | 1 ... 16                                   |        |        |        |
| Offset                  | Channel member offset  |               |        | 0, 16, 32 ... to access up to 255 channels |        |        |        |
| VctCoefficient          | DATA_0 to DATA_3 [V/K] |               |        | R4                                         |        |        |        |

Table 87: vct coefficient

### 3.5.1.25 Temperature external<sup>4</sup> (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID       | CHN    | DATA_3                                     | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|---------------|--------|--------------------------------------------|--------|--------|--------|
| master read -           | 1                     | 0x4121        | Mx     |                                            |        |        |        |
| master single MBR read- | 1                     | 0x6121        | Member |                                            | Offset |        |        |
| HV board write access   | 0                     | 0x4121/0x6121 | Mx     | TemperatureExternal                        |        |        |        |
| Notes:                  |                       |               |        |                                            |        |        |        |
| Mx                      | Channel               |               |        | 0 ... 255                                  |        |        |        |
| Member                  | Members               |               |        | 1 ... 16                                   |        |        |        |
| Offset                  | Channel member offset |               |        | 0, 16, 32 ... to access up to 255 channels |        |        |        |
| TemperatureExternal     | DATA_0 to DATA_3 [°C] |               |        | R4                                         |        |        |        |

Table 88: temperature external

<sup>3</sup> Option VCT only

<sup>4</sup> Option VCT only

### 3.5.1.26 Resistor external<sup>5</sup> (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID       | CHN                                        | DATA_3           | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|---------------|--------------------------------------------|------------------|--------|--------|--------|
| master write access     | 0                     | 0x4122        | MX                                         | ResistorExternal |        |        |        |
| master read -           | 1                     | 0x4122        | Mx                                         |                  |        |        |        |
| master single MBR read- | 1                     | 0x6122        | Member                                     |                  | Offset |        |        |
| HV board write access   | 0                     | 0x4122/0x6122 | Mx                                         | ResistorExternal |        |        |        |
| Notes:                  |                       |               |                                            |                  |        |        |        |
| Mx                      | Channel               |               | 0 ... 255                                  |                  |        |        |        |
| Member                  | Members               |               | 1 ... 16                                   |                  |        |        |        |
| Offset                  | Channel member offset |               | 0, 16, 32 ... to access up to 255 channels |                  |        |        |        |
| ResistorExternal        | DATA_0 to DATA_3 [Ω]  |               | R4                                         |                  |        |        |        |

Table 89: resistors external

### 3.5.1.27 VoltageRampSpeedUp (single write- / single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR               | DATA_ID         | CHN                                             | DATA_3             | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|------------------------|-----------------|-------------------------------------------------|--------------------|--------|--------|--------|
| master write access     | 0                      | 0x4123          | MX                                              | VoltageRampSpeedUp |        |        |        |
| master read -           | 1                      | 0x4123          | MX                                              |                    |        |        |        |
| master single MBR read- | 1                      | 0x6123          | Member                                          |                    | Offset |        |        |
| HV board write access   | 0                      | 0x4123 / 0x6123 | MX                                              | VoltageRampSpeedUp |        |        |        |
| Notes:                  |                        |                 |                                                 |                    |        |        |        |
| Mx                      | Channel                |                 | 0 ... 255                                       |                    |        |        |        |
| Member                  | Members                |                 | 1 ... 16                                        |                    |        |        |        |
| Offset                  | Channel member offset  |                 | 0, 16, 32 ... to access up to 255 channels      |                    |        |        |        |
| VoltageRampSpeedUp      | DATA_0 to DATA_3 [V/s] |                 | R4 (VoltageRampSpeedMin to VoltageRampSpeedMax) |                    |        |        |        |

Table 90: voltage ramp speed

<sup>5</sup> Option EHS STACK

### 3.5.1.28 VoltageRampSpeedDown (single write- / single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR               | DATA_ID         | CHN                                             | DATA_3               | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|------------------------|-----------------|-------------------------------------------------|----------------------|--------|--------|--------|
| master write access     | 0                      | 0x4124          | MX                                              | VoltageRampSpeedDown |        |        |        |
| master read -           | 1                      | 0x4124          | MX                                              |                      |        |        |        |
| master single MBR read- | 1                      | 0x6124          | Member                                          |                      | Offset |        |        |
| HV board write access   | 0                      | 0x4124 / 0x6124 | MX                                              | VoltageRampSpeedDown |        |        |        |
| Notes:                  |                        |                 |                                                 |                      |        |        |        |
| Mx                      | Channel                |                 | 0 ... 255                                       |                      |        |        |        |
| Member                  | Members                |                 | 1 ... 16                                        |                      |        |        |        |
| Offset                  | Channel member offset  |                 | 0, 16, 32 ... to access up to 255 channels      |                      |        |        |        |
| VoltageRampSpeedDown    | DATA_0 to DATA_3 [V/s] |                 | R4 (VoltageRampSpeedMin to VoltageRampSpeedMax) |                      |        |        |        |

Table 91: voltage ramp speed down

### 3.5.1.29 CurrentRampSpeedUp (single write- / single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR               | DATA_ID         | CHN                                             | DATA_3             | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|------------------------|-----------------|-------------------------------------------------|--------------------|--------|--------|--------|
| master write access     | 0                      | 0x4123          | MX                                              | CurrentRampSpeedUp |        |        |        |
| master read -           | 1                      | 0x4123          | MX                                              |                    |        |        |        |
| master single MBR read- | 1                      | 0x6123          | Member                                          |                    | Offset |        |        |
| HV board write access   | 0                      | 0x4123 / 0x6123 | MX                                              | CurrentRampSpeedUp |        |        |        |
| Notes:                  |                        |                 |                                                 |                    |        |        |        |
| Mx                      | Channel                |                 | 0 ... 255                                       |                    |        |        |        |
| Member                  | Members                |                 | 1 ... 16                                        |                    |        |        |        |
| Offset                  | Channel member offset  |                 | 0, 16, 32 ... to access up to 255 channels      |                    |        |        |        |
| CurrentRampSpeedUp      | DATA_0 to DATA_3 [A/s] |                 | R4 (CurrentRampSpeedMin to CurrentRampSpeedMax) |                    |        |        |        |

Table 92: current ramp speed up

### 3.5.1.30 CurrentRampSpeedDown (single write- / single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR               | DATA_ID         | CHN                                             | DATA_3               | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|------------------------|-----------------|-------------------------------------------------|----------------------|--------|--------|--------|
| master write access     | 0                      | 0x4124          | MX                                              | CurrentRampSpeedDown |        |        |        |
| master read -           | 1                      | 0x4124          | MX                                              |                      |        |        |        |
| master single MBR read- | 1                      | 0x6124          | Member                                          |                      | Offset |        |        |
| HV board write access   | 0                      | 0x4124 / 0x6124 | MX                                              | CurrentRampSpeedDown |        |        |        |
| Notes:                  |                        |                 |                                                 |                      |        |        |        |
| Mx                      | Channel                |                 | 0 ... 255                                       |                      |        |        |        |
| Member                  | Members                |                 | 1 ... 16                                        |                      |        |        |        |
| Offset                  | Channel member offset  |                 | 0, 16, 32 ... to access up to 255 channels      |                      |        |        |        |
| VoltageRampSpeedDown    | DATA_0 to DATA_3 [A/s] |                 | R4 (CurrentRampSpeedMin to CurrentRampSpeedMax) |                      |        |        |        |

Table 93: current speed down

### 3.5.1.31 VoltageRampSpeedMin (single write- / single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR               | DATA_ID         | CHN                                        | DATA_3              | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|------------------------|-----------------|--------------------------------------------|---------------------|--------|--------|--------|
| master write access     | 0                      | 0x4127          | MX                                         | VoltageRampSpeedMin |        |        |        |
| master read -           | 1                      | 0x4127          | MX                                         |                     |        |        |        |
| master single MBR read- | 1                      | 0x6127          | Member                                     |                     | Offset |        |        |
| HV board write access   | 0                      | 0x4127 / 0x6127 | MX                                         | VoltageRampSpeedMin |        |        |        |
| Notes:                  |                        |                 |                                            |                     |        |        |        |
| Mx                      | Channel                |                 | 0 ... 255                                  |                     |        |        |        |
| Member                  | Members                |                 | 1 ... 16                                   |                     |        |        |        |
| Offset                  | Channel member offset  |                 | 0, 16, 32 ... to access up to 255 channels |                     |        |        |        |
| VoltageRampSpeedMin     | DATA_0 to DATA_3 [V/s] |                 | R4                                         |                     |        |        |        |

Table 94: voltage ramp speed min

### 3.5.1.32 VoltageRampSpeedMax (single write- / single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR               | DATA_ID         | CHN                                        | DATA_3              | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|------------------------|-----------------|--------------------------------------------|---------------------|--------|--------|--------|
| master write access     | 0                      | 0x4128          | MX                                         | VoltageRampSpeedMax |        |        |        |
| master read -           | 1                      | 0x4128          | MX                                         |                     |        |        |        |
| master single MBR read- | 1                      | 0x6128          | Member                                     |                     | Offset |        |        |
| HV board write access   | 0                      | 0x4128 / 0x6128 | MX                                         | VoltageRampSpeedMax |        |        |        |
| Notes:                  |                        |                 |                                            |                     |        |        |        |
| Mx                      | Channel                |                 | 0 ... 255                                  |                     |        |        |        |
| Member                  | Members                |                 | 1 ... 16                                   |                     |        |        |        |
| Offset                  | Channel member offset  |                 | 0, 16, 32 ... to access up to 255 channels |                     |        |        |        |
| VoltageRampSpeedMax     | DATA_0 to DATA_3 [V/s] |                 | R4                                         |                     |        |        |        |

Table 95: voltages ramp speed max

### 3.5.1.33 CurrentRampSpeedMin (single write- / single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR               | DATA_ID         | CHN                                        | DATA_3              | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|------------------------|-----------------|--------------------------------------------|---------------------|--------|--------|--------|
| master write access     | 0                      | 0x4129          | MX                                         | CurrentRampSpeedMin |        |        |        |
| master read -           | 1                      | 0x4129          | MX                                         |                     |        |        |        |
| master single MBR read- | 1                      | 0x6129          | Member                                     |                     | Offset |        |        |
| HV board write access   | 0                      | 0x4129 / 0x6129 | MX                                         | CurrentRampSpeedMin |        |        |        |
| Notes:                  |                        |                 |                                            |                     |        |        |        |
| Mx                      | Channel                |                 | 0 ... 255                                  |                     |        |        |        |
| Member                  | Members                |                 | 1 ... 16                                   |                     |        |        |        |
| Offset                  | Channel member offset  |                 | 0, 16, 32 ... to access up to 255 channels |                     |        |        |        |
| CurrentRampSpeedMin     | DATA_0 to DATA_3 [A/s] |                 | R4                                         |                     |        |        |        |

Table 96: current ramp speed min

### 3.5.1.34 CurrentRampSpeedMax (single write- / single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR               | DATA_ID         | CHN                                        | DATA_3              | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|------------------------|-----------------|--------------------------------------------|---------------------|--------|--------|--------|
| master write access     | 0                      | 0x4130          | MX                                         | CurrentRampSpeedMax |        |        |        |
| master read -           | 1                      | 0x4130          | MX                                         |                     |        |        |        |
| master single MBR read- | 1                      | 0x6130          | Member                                     |                     | Offset |        |        |
| HV board write access   | 0                      | 0x4130 / 0x6130 | MX                                         | CurrentRampSpeedMax |        |        |        |
| Notes:                  |                        |                 |                                            |                     |        |        |        |
| Mx                      | Channel                |                 | 0 ... 255                                  |                     |        |        |        |
| Member                  | Members                |                 | 1 ... 16                                   |                     |        |        |        |
| Offset                  | Channel member offset  |                 | 0, 16, 32 ... to access up to 255 channels |                     |        |        |        |
| CurrentRampSpeedMax     | DATA_0 to DATA_3 [A/s] |                 | R4                                         |                     |        |        |        |

Table 97: current ramp speed max

### 3.5.1.35 PowerSet (single write- / single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID         | CHN                                        | DATA_3   | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|-----------------|--------------------------------------------|----------|--------|--------|--------|
| master write access     | 0                     | 0x4134          | MX                                         | PowerSet |        |        |        |
| master read -           | 1                     | 0x4134          | MX                                         |          |        |        |        |
| master single MBR read- | 1                     | 0x6134          | Member                                     |          | Offset |        |        |
| HV board write access   | 0                     | 0x4134 / 0x6134 | MX                                         | PowerSet |        |        |        |
| Notes:                  |                       |                 |                                            |          |        |        |        |
| Mx                      | Channel               |                 | 0 ... 255                                  |          |        |        |        |
| Member                  | Members               |                 | 1 ... 16                                   |          |        |        |        |
| Offset                  | Channel member offset |                 | 0, 16, 32 ... to access up to 255 channels |          |        |        |        |
| PowerSet                | DATA_0 to DATA_3 [W]  |                 | R4                                         |          |        |        |        |

Table 98: power set

### 3.5.1.36 PowerMeasure (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID         | CHN                                        | DATA_3       | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|-----------------|--------------------------------------------|--------------|--------|--------|--------|
| master read -           | 1                     | 0x4135          | MX                                         |              |        |        |        |
| master single MBR read- | 1                     | 0x6135          | Member                                     |              | Offset |        |        |
| HV board write access   | 0                     | 0x4135 / 0x6135 | MX                                         | PowerMeasure |        |        |        |
| Notes:                  |                       |                 |                                            |              |        |        |        |
| Mx                      | Channel               |                 | 0 ... 255                                  |              |        |        |        |
| Member                  | Members               |                 | 1 ... 16                                   |              |        |        |        |
| Offset                  | Channel member offset |                 | 0, 16, 32 ... to access up to 255 channels |              |        |        |        |
| PowerMeasure            | DATA_0 to DATA_3 [W]  |                 | R4                                         |              |        |        |        |

Table 99: power measure

### 3.5.1.37 Output mode<sup>6</sup> (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID       | CHN                                        | DATA_0 |
|-------------------------|-----------------------|---------------|--------------------------------------------|--------|
| master write access     | 0                     | 0x4140        | Mx                                         | Mode   |
| master read -           | 1                     | 0x4140        | Mx                                         |        |
| master single MBR read- | 1                     | 0x6140        | Member                                     | Offset |
| HV board write access   | 0                     | 0x4120/0x6120 | Mx                                         | Mode   |
| Notes:                  |                       |               |                                            |        |
| Mx                      | Channel               |               | 0 ... 255                                  |        |
| Member                  | Members               |               | 1 ... 16                                   |        |
| Offset                  | Channel member offset |               | 0, 16, 32 ... to access up to 255 channels |        |
| Mode                    | DATA_0                |               | UI1 (HV MODE = 1, 2 or 3)                  |        |

Table 100: output mode

<sup>6</sup> Option HV-MODE SWITCHABLE

### 3.5.1.38 Output polarity<sup>7</sup> (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID                                    | CHN    | DATA_0   |
|-------------------------|-----------------------|--------------------------------------------|--------|----------|
| master write access     | 0                     | 0x4141                                     | Mx     | Polarity |
| master read -           | 1                     | 0x4141                                     | Mx     |          |
| master single MBR read- | 1                     | 0x6141                                     | Member | Offset   |
| HV board write access   | 0                     | 0x4121/0x6121                              | Mx     | Polarity |
| Notes:                  |                       |                                            |        |          |
| Mx                      | Channel               | 0 ... 255                                  |        |          |
| Member                  | Members               | 1 ... 16                                   |        |          |
| Offset                  | Channel member offset | 0, 16, 32 ... to access up to 255 channels |        |          |
| Polarity                | DATA_0                | SI1 (Positive = +1, Negative = -1)         |        |          |

Table 101: output polarity

### 3.5.1.39 Output voltage mode<sup>8</sup> (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID       | CHN                                             | DATA_3      | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|---------------|-------------------------------------------------|-------------|--------|--------|--------|
| master read -           | 1                     | 0x4142        | Mx                                              |             |        |        |        |
| master single MBR read- | 1                     | 0x6142        | Member                                          |             | Offset |        |        |
| HV board write access   | 0                     | 0x4142/0x6142 | Mx                                              | VoltageMode |        |        |        |
| Notes:                  |                       |               |                                                 |             |        |        |        |
| Mx                      | Channel               |               | 0 ... 255                                       |             |        |        |        |
| Member                  | Members               |               | 1 ... 16                                        |             |        |        |        |
| Offset                  | Channel member offset |               | 0, 16, 32 ... to access up to 255 channels      |             |        |        |        |
| VoltageMode             | DATA_0 to DATA_3 [V]  |               | R4 (+6000, +4000, +2000, -2000, -4000 or -6000) |             |        |        |        |

Table 102: voltage mode

<sup>7</sup> Option POLARITY SWITCHABLE

<sup>8</sup> Option HV-MODE SWITCHABLE

### 3.5.1.40 Output current mode<sup>9</sup> (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID                                                                      | CHN    | DATA_3      | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|------------------------------------------------------------------------------|--------|-------------|--------|--------|--------|
| master read -           | 1                     | 0x4143                                                                       | Mx     |             |        |        |        |
| master single MBR read- | 1                     | 0x6143                                                                       | Member |             | Offset |        |        |
| HV board write access   | 0                     | 0x4143/0x6143                                                                | Mx     | CurrentMode |        |        |        |
| Notes:                  |                       |                                                                              |        |             |        |        |        |
| Mx                      | Channel               | 0 ... 255                                                                    |        |             |        |        |        |
| Member                  | Members               | 1 ... 16                                                                     |        |             |        |        |        |
| Offset                  | Channel member offset | 0, 16, 32 ... to access up to 255 channels                                   |        |             |        |        |        |
| CurrentMode             | DATA_0 to DATA_3 [A]  | R4 (+4.0E-3, +3.0E-3, +2.0E-3, +0.1E-3, -0.1E-3,-2.0E-3, -3.0E-3 or -4.0E-3) |        |             |        |        |        |

Table 103: output current mode

### 3.5.1.41 Output voltage mode list<sup>10</sup> (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID         | CHN                                             | DATA_3          | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|-----------------|-------------------------------------------------|-----------------|--------|--------|--------|
| master read -           | 1                     | 0x4150 - 0x415f | Mx                                              |                 |        |        |        |
| master single MBR read- | 1                     | 0x6150 - 0x415f | Member                                          |                 | Offset |        |        |
| HV board write access   | 0                     | 0x4150/0x6150   | Mx                                              | VoltageModeList |        |        |        |
| Notes:                  |                       |                 |                                                 |                 |        |        |        |
| Mx                      | Channel               |                 | 0 ... 255                                       |                 |        |        |        |
| Member                  | Members               |                 | 1 ... 16                                        |                 |        |        |        |
| Offset                  | Channel member offset |                 | 0, 16, 32 ... to access up to 255 channels      |                 |        |        |        |
| VoltageModeList         | DATA_0 to DATA_3 [V]  |                 | R4 (+6000, +4000, +2000, -2000, -4000 or -6000) |                 |        |        |        |

Table 104: output voltage mode list

### 3.5.1.42 Output current mode list<sup>11</sup> (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR              | DATA_ID       | CHN                                                                           | DATA_3      | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|-----------------------|---------------|-------------------------------------------------------------------------------|-------------|--------|--------|--------|
| master read -           | 1                     | 0x4143        | Mx                                                                            |             |        |        |        |
| master single MBR read- | 1                     | 0x6143        | Member                                                                        |             | Offset |        |        |
| HV board write access   | 0                     | 0x4143/0x6143 | Mx                                                                            | CurrentMode |        |        |        |
| Notes:                  |                       |               |                                                                               |             |        |        |        |
| Mx                      | Channel               |               | 0 ... 255                                                                     |             |        |        |        |
| Member                  | Members               |               | 1 ... 16                                                                      |             |        |        |        |
| Offset                  | Channel member offset |               | 0, 16, 32 ... to access up to 255 channels                                    |             |        |        |        |
| VoltageMode             | DATA_0 to DATA_3 [A]  |               | R4 (+4.0E-3, +3.0E-3, +2.0E-3, +0.1E-3, -0.1E-3,-2.0E-3, -3.0E-3 or - 4.0E-3) |             |        |        |        |

Table 105: output current mode list

<sup>9</sup> Option HV-MODE SWITCHABLE

<sup>10</sup> Option HV-MODE SWITCHABLE

<sup>11</sup> Option HV-MODE SWITCHABLE

### 3.5.1.43 Group number (single/ multiple single read-write access)

EDCP frame:

| Access                  | DATA_DIR | DATA_ID                             | CHN    | DATA_0                                     |        |       |
|-------------------------|----------|-------------------------------------|--------|--------------------------------------------|--------|-------|
| master write access     | 0        | 0x4200                              | Mx     | GROUP                                      |        |       |
| master read -           | 1        | 0x4200                              | Mx     |                                            |        |       |
| master single MBR read- | 1        | 0x6200                              | Member |                                            | Offset | GROUP |
| HV board write access   | 0        | 0x4200                              | Mx     | GROUP                                      |        |       |
| Notes:                  |          |                                     |        |                                            |        |       |
| Mx                      |          | Channel                             |        | 0 ... 255                                  |        |       |
| Member                  |          | Members                             |        | 1 ... 16                                   |        |       |
| Offset                  |          | Channel member offset               |        | 0, 16, 32 ... to access up to 255 channels |        |       |
| Group                   |          | Group number of the channel members |        | 0 .. 255                                   |        |       |

Table 106: group number

With a group number GROUP for each channel, channels can be combined to groups involving all connected modules. The NMT channel group set and the NMT module set frames (described on page 44) send broadcast information for all channels, which have the same group number.

## 3.5.2 EDCP Module Accesses

### 3.5.2.1 ModuleStatus (module read-write access)

EDCP frame:

| Access                | DATA_DIR         | DATA_ID | DATA_1       | DATA_0 |
|-----------------------|------------------|---------|--------------|--------|
| master read-          | 1                | 0x1000  |              |        |
| HV board write access | 0                | 0x1000  | ModuleStatus |        |
| Notes:                |                  |         |              |        |
| ModuleStatus          | DATA_0 to DATA_1 | UI2     |              |        |

Table 107

| Bit15        | Bit14              | Bit13                        | Bit12        | Bit11            | Bit10             | Bit09    | Bit08        |
|--------------|--------------------|------------------------------|--------------|------------------|-------------------|----------|--------------|
| isKillEnable | isTemperature Good | isSupplyGood                 | isModuleGood | isEvtActive      | isSafetyLoop Good | isNoRamp | isNoSumError |
| Bit07        | Bit06              | Bit05                        | Bit04        | Bit03            | Bit02             | Bit01    | Bit00        |
| Reserved     | isInputError       | isHardware VoltageLimit Good | needService  | isHighVoltage On | isLiveInsertion   | Reserved | isAdjust     |

Table 108

### 3.5.2.2 ModuleStatus32 (module read-write access)

EDCP frame:

| Access                                                                | DATA_DIR | DATA_ID | DATA_3         | DATA_2 | DATA_1 | DATA_0 |
|-----------------------------------------------------------------------|----------|---------|----------------|--------|--------|--------|
| master read-                                                          | 1        | 0x1080  |                |        |        |        |
| HV board write access                                                 | 0        | 0x1080  | ModuleStatus32 |        |        |        |
| Notes:<br>ModuleStatus32    DATA_0 to DATA_4                      UI4 |          |         |                |        |        |        |

Table 109

| Bit31        | Bit30               | Bit29                         | Bit28         | Bit27             | Bit26             | Bit25    | Bit24                |
|--------------|---------------------|-------------------------------|---------------|-------------------|-------------------|----------|----------------------|
| Reserved     | Reserved            | Reserved                      | Reserved      | Reserved          | Reserved          | Reserved | Reserved             |
| Bit23        | Bit22               | Bit21 <sup>(1)</sup>          | Bit20         | Bit19             | Bit18             | Bit17    | Bit16 <sup>(1)</sup> |
| Reserved     | Reserved            | is Voltage Ramp Speed Limited | Reserved      | Reserved          | Reserved          | Reserved | is Fast Ramp Down    |
| Bit15        | Bit14               | Bit13                         | Bit12         | Bit11             | Bit10             | Bit09    | Bit08                |
| isKillEnable | is Temperature Good | isSupplyGood                  | isModule Good | isEvent Active    | isSafetyLoop Good | isNoRamp | isNoSum Error        |
| Bit07        | Bit06               | Bit05                         | Bit04         | Bit03             | Bit02             | Bit01    | Bit00                |
| Reserved     | is Input Error      | isHardware VoltageLimit Good  | needService   | isHigh Voltage On | isLiveInsertion   | Reserved | is Fine Adjustment   |

Table 110

The status bit `IsCommandComplete` indicates whether all CAN commands given to the module have been executed.

| Bit               | Name | Description                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| isKillEnable      |      | Module state of kill enable<br><br>isKillEnable=0      Module in state kill disable<br>isKillEnable=1      Module in state kill enable                                                                                                                                                                                                                                                                                       |
| isTemperatureGood |      | Module temperature good<br><br>isTemperatureGood=0      If module temperature is higher than 55°C then all channel are switched off permanently<br>isTemperatureGood=1      module temperature is within working range                                                                                                                                                                                                       |
| isSupplyGood      |      | Power supply good<br><br>isSupplyGood=0      supply voltages are out of range (range of 24V +/-10% and of 5V +/-5%)<br>isSupplyGood=1      supply voltages are within range                                                                                                                                                                                                                                                  |
| isModuleGood      |      | Module in state good<br><br>isModuleGood=0    module is not good, that means (isnoSERR AND (ETMPngd OR ESPLYngd OR ESFLPngd))==0<br>isModuleGood=1    module is good, that means (isnoSERR AND NOT(ETMPngd OR ESPLYngd OR ESFLPngd))==1 (see module event status also)                                                                                                                                                       |
| isEventActive     |      | Any event is active and mask is set<br><br>isEventActive=0    no Event is active<br>isEventActive=1    any Event is active                                                                                                                                                                                                                                                                                                   |
| isSafetyLoopGood  |      | Safety loop closed<br><br>isSafetyLoopGood=0      safety loop is broken -VO has been shut off,<br>isSafetyLoopGood=1      safety loop is closed                                                                                                                                                                                                                                                                              |
| isNoRamp          |      | All channels stable, no ramp active<br><br>isNoRamp=0 voltage output is ramping in at least one channel<br>isNoRamp=1 no channel is ramping                                                                                                                                                                                                                                                                                  |
| isNoSumError      |      | All channels without failure<br><br>isNoSumError=0    voltage limit, current limit, trip, voltage bound or current bound has been exceeded in at least one of the channels or external INHIBIT<br>→ error, reset by reset of the corresponding flag of the ‘channel status’<br>isnoSumERR=1      evaluation of the ‘Channel Status’ over all channels to a sum error flag<br>→ LIM&CLIM&CTRP&EINH&VBND&CBND=0<br>→ no errors |

| Bit                        | Name | Description                                                                                                                                                                                                                                                 |
|----------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| isInputError               |      | Input error in connection with a module access<br><br>isInputError=1      input error in connection with a module access<br>isInputError=0      no input error in connection with a module access                                                           |
| isHardwareVoltageLimitGood |      | Hardware voltage limit in proper range, for HV distributor modules with current mirror only<br><br>isHardwareVoltageLimitGood=0      hardware voltage limit not in proper range<br>isHardwareVoltageLimitGood=1      hardware voltage limit in proper range |
| isServiceNeeded            |      | Hardware failure detected (consult iseg Spezialelektronik GmbH)<br><br>isServiceNeeded=0 Module is ready for working<br>isServiceNeeded=1 Module need a service                                                                                             |
| isHighVoltageOn            |      | At least one channel generates a high voltage<br><br>isHighVoltageOn=0 No high voltage will be generated<br>isHighVoltageOn=1 At least one channel generates a high voltage output.<br><br>(Modules with 7 digit serial number only.)                       |
| isLiveInsertion            |      | Mode live insertion<br><br>isLiveInsertion=0      no Live Insertion mode<br>isLiveInsertion=1      Live Insertion mode                                                                                                                                      |
| isFineAdjustment           |      | Mode of the fine adjustment<br><br>isFineAdjustment=0      Fine adjustment is off.<br>isFineAdjustment=1      Fine adjustment is on (default).                                                                                                              |
| Reserved                   |      |                                                                                                                                                                                                                                                             |

Table 111

### 3.5.2.3 ModuleControl (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR                       | DATA_ID | DATA_1        | DATA_0 |
|-----------------------|--------------------------------|---------|---------------|--------|
| master write access   | 0                              | 0x1001  | ModuleControl |        |
| master read-          | 1                              | 0x1001  |               |        |
| HV board write access | 0                              | 0x1001  | ModuleControl |        |
| Notes:                |                                |         |               |        |
| ModuleControl         | DATA_0 to DATA_1 ( Bit 0 -15 ) |         | UI2           |        |

Table 112

### 3.5.2.4 ModuleControl32 (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR                     | DATA_ID | DATA_3          | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|------------------------------|---------|-----------------|--------|--------|--------|
| master write          | 0                            | 0x1081  | ModuleControl32 |        |        |        |
| master read-          | 1                            | 0x1081  |                 |        |        |        |
| HV board write access | 0                            | 0x1081  | ModuleControl32 |        |        |        |
| Notes:                |                              |         |                 |        |        |        |
| ModuleControl32       | DATA_0 to DATA_3 (Bit 0 -31) |         |                 | UI4    |        |        |

Table 113

| Bit31       | Bit30          | Bit29        | Bit28              | Bit27        | Bit26    | Bit25          | Bit24                          |
|-------------|----------------|--------------|--------------------|--------------|----------|----------------|--------------------------------|
| Reserved    | Reserved       | Reserved     | Reserved           | Reserved     | Reserved | Reserved       | Reserved                       |
| Bit23       | Bit22          | Bit21        | Bit20              | Bit19        | Bit18    | Bit17          | Bit16                          |
| Reserved    | Reserved       | Reserved     | Reserved           | Reserved     | Reserved | setRelay Three | disable VoltageRamp SpeedLimit |
| Bit15       | Bit14          | Bit13        | Bit12              | Bit11        | Bit10    | Bit09          | Bit08                          |
| Reserved    | set KillEnable | setR2        | setFine Adjustment | setBigEndian | Reserved | Reserved       | Reserved                       |
| Bit07       | Bit06          | Bit05        | Bit04              | Bit03        | Bit02    | Bit01          | Bit00                          |
| setRelayOne | doClear        | setInterlock | doMultiplex        | Reserved     | Reserved | Reserved       | Reserved                       |

Table 114

| Bit                          | Description                                                                                                                                                                                                                                                                                           |
|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| setRelayThree                |                                                                                                                                                                                                                                                                                                       |
| disableVoltageRampSpeedLimit | Switch off voltage ramp speed limitation                                                                                                                                                                                                                                                              |
| killEnable                   | Kill function<br>SetKILL = 0      kill function disable<br>setKILL = 1      kill function enable                                                                                                                                                                                                      |
| adjust                       | Switch ON of fine adjustment<br>setADJ = 0      fine adjustment OFF<br>setADJ = 1      fine adjustment ON                                                                                                                                                                                             |
| setBigEndian                 | Order of bytes in word: 0 = Little Endian (INTEL); 1 = Big Endian (MOTOROLA)<br>setENDN = 1      big endian (MOTOROLA format)                                                                                                                                                                         |
| clearKill                    | Hardware ClearKill signal and clear all event signals of module and channels<br>doCLEAR =1      Hardware ClearKill signal and clear all event signals of the module and the channels<br>doCLEAR=0      no action                                                                                      |
| Interlock                    | Interlock signal CRATE_ENABLE (WIENER MPOD crate, active TTL high)<br>setILK= 1      INTERLOCK signal in order to switch off HV and set bit EEINH of the EventStatus for all channels<br>setILK=0      reset the INTERLOCK signal in order to clear the bit EEINH of the EventStatus for all channels |
| doMultiplex                  | Switch on multiplexing, for electronic load (EZL) only                                                                                                                                                                                                                                                |
|                              | doMux = 0      switch off multiplexing<br>doMux = 1      switch on multiplexing                                                                                                                                                                                                                       |
| setRelayOne                  | Switch on load one, for electronic load (EZL) only                                                                                                                                                                                                                                                    |
|                              |                                                                                                                                                                                                                                                                                                       |
| setRelayTwo                  | Switch on load two, for electronic load (EZL) only                                                                                                                                                                                                                                                    |
|                              | setR1/2/3 = 0      switch off load 1, 2 or 3<br>setR1/2/3 = 1      switch on load 1, 2 or 3                                                                                                                                                                                                           |
| Reserved                     |                                                                                                                                                                                                                                                                                                       |

Table 115

### 3.5.2.5 ModuleEventStatus (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR | DATA_ID          | DATA_1            | DATA_0 |
|-----------------------|----------|------------------|-------------------|--------|
| master write          | 0        | 0x1002           | ModuleEventStatus |        |
| master read-          | 1        | 0x1002           |                   |        |
| HV board write access | 0        | 0x1002           | ModuleEventStatus |        |
| Notes:                |          |                  |                   |        |
| ModuleEventStatus     |          | DATA_0 to DATA_1 | UI2               |        |

Table 116

### 3.5.2.6 ModuleEventStatus32 (single/ multiple single read-write access)

EDCP frame:

| Access                | DATA_DIR | DATA_ID          | DATA_3              | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------|------------------|---------------------|--------|--------|--------|
| master write          | 0        | 0x1082           | ModuleEventStatus32 |        |        |        |
| master read-          | 1        | 0x1082           |                     |        |        |        |
| HV board write access | 0        | 0x1082           | ModuleEventStatus32 |        |        |        |
| Notes:                |          |                  |                     |        |        |        |
| ModuleEventStatus     |          | DATA_0 to DATA_1 | UI2                 |        |        |        |

Table 117

| Bit31    | Bit30                      | Bit29                                 | Bit28         | Bit27    | Bit26                      | Bit25    | Bit24    |
|----------|----------------------------|---------------------------------------|---------------|----------|----------------------------|----------|----------|
| Reserved | Reserved                   | Reserved                              | Reserved      | Reserved | Reserved                   | Reserved | Reserved |
| Bit23    | Bit22                      | Bit21                                 | Bit20         | Bit19    | Bit18                      | Bit17    | Bit16    |
| Reserved | Reserved                   | Reserved                              | Reserved      | Reserved | Reserved                   | Reserved | Reserved |
| Bit15    | Bit14                      | Bit13                                 | Bit12         | Bit11    | Bit10                      | Bit09    | Bit08    |
| Reserved | Event Temperature Not Good | Event Supply Not Good                 | Reserved      | Reserved | Event Safety Loop Not Good | Reserved | Reserved |
| Bit07    | Bit06                      | Bit05                                 | Bit04         | Bit03    | Bit02                      | Bit01    | Bit00    |
| Reserved | Event Input Error          | Event Hardware Voltage Limit Not Good | Event Service | Reserved | Event Live Insertion       | Reserved | Reserved |

Table 118

| Bit      | Name                                  | Description                                                                                                                                                                     |
|----------|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ETMPngd  | Event Temperature Not Good            | Event: Temperature is above 55°C                                                                                                                                                |
| ESPLYngd | Event Supply Not Good                 | Event: at least one of the supplies is not good                                                                                                                                 |
| ESFLPngd | Event Safety Loop Not Good            | Event: Safety loop is open                                                                                                                                                      |
| EIERR    | Event Input Error                     | Event: input error in connection with a module access                                                                                                                           |
| EHwVLngd | Event Hardware Voltage Limit Not Good | Event: Hardware voltage limit is not in proper range, only for HV distributor modules with current mirror;                                                                      |
| ESrvs    | Event Service                         | Event: A hardware failure of the HV module has been detected. The HV will switched off without a possibility to switch on again. Please consult the iseg Spzialelektronik GmbH. |
| ELVINS   | Event Live Insertion                  | Event live insertion to prepare a hot plug of a module                                                                                                                          |
| res      | Reserved                              |                                                                                                                                                                                 |

Table 119

### 3.5.2.7 ModuleEventMask (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR         | DATA_ID | DATA_1          | DATA_0 |
|-----------------------|------------------|---------|-----------------|--------|
| master write          | 0                | 0x1003  | ModuleEventMask |        |
| master read-          | 1                | 0x1003  |                 |        |
| HV board write access | 0                | 0x1003  | ModuleEventMask |        |
| Notes:                |                  |         |                 |        |
| ModuleEventMask       | DATA_0 to DATA_1 |         | UI2             |        |

Table 120

### 3.5.2.8 ModuleEventMask32 (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR         | DATA_ID | DATA_3            | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|------------------|---------|-------------------|--------|--------|--------|
| master write          | 0                | 0x1083  | ModuleEventMask32 |        |        |        |
| master read-          | 1                | 0x1083  |                   |        |        |        |
| HV board write access | 0                | 0x1083  | ModuleEventMask32 |        |        |        |
| Notes:                |                  |         |                   |        |        |        |
| ModuleEventMask32     | DATA_0 to DATA_3 |         | UI3               |        |        |        |

Table 121

| Bit31    | Bit30                           | Bit29                                      | Bit28    | Bit27    | Bit26                           | Bit25    | Bit24    |
|----------|---------------------------------|--------------------------------------------|----------|----------|---------------------------------|----------|----------|
| Reserved | Reserved                        | Reserved                                   | Reserved | Reserved | Reserved                        | Reserved | Reserved |
| Bit23    | Bit22                           | Bit21                                      | Bit20    | Bit19    | Bit18                           | Bit17    | Bit16    |
| Reserved | Reserved                        | Reserved                                   | Reserved | Reserved | Reserved                        | Reserved | Reserved |
| Bit15    | Bit14                           | Bit13                                      | Bit12    | Bit11    | Bit10                           | Bit09    | Bit08    |
| Reserved | Mask Event Temperature Not Good | Mask Event Supply Not Good                 | Reserved | Reserved | Mask Event Safety Loop Not Good | Reserved | Reserved |
| Bit07    | Bit06                           | Bit05                                      | Bit04    | Bit03    | Bit02                           | Bit01    | Bit00    |
| Reserved | Mask Event Input Error          | Mask Event Hardware Voltage Limit Not Good | Reserved | Reserved | Reserved                        | Reserved | Reserved |

Table 122

| Bit       | Name                                       | Description                                                                                                     |
|-----------|--------------------------------------------|-----------------------------------------------------------------------------------------------------------------|
| METMPngd  | Mask Event Temperature Not Good            | MEventMask: Temperature is above 55°C                                                                           |
| MESPLYngd | Mask Event Supply Not Good                 | MEventMask: at least one of the supplies is not good                                                            |
| MESFLPngd | Mask Event Safety Loop Not Good            | MEventMask: Safety loop (SL) is open                                                                            |
| MEIERR    | Mask Event Input Error                     | MEventMask: Input error in connection with a module access                                                      |
| MEHWLNgd  | Mask Event Hardware Voltage Limit Not Good | MEventMask: Hardware voltage limit is not in proper range, only for HV distributor modules with current mirror; |
| Reserved  | Reserved                                   |                                                                                                                 |

Table 123

All bits of the EventMask register are set to “0” after the power on reset.

Module in mode KILL enable: If a bit of the EventStatus register is set to “1” and the corresponding bit in the EventMask register is “0” no reset of the EventStatus bits is necessary before switch on the HV of any channel again.

If a bit of the EventMask register is set to “1” and if the corresponding bit in the EventStatus is set to “1” by the module firmware a reset of the corresponding EventStatus bits is necessary before a switch on the HV of any channel is possible.

Module in mode KILL enable: A reset of the EventStatus bits is necessary before switch on the HV of any channel is possible.

### 3.5.2.9 ModuleEventChannelStatus (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR                    | DATA_ID | DATA_2                                  | DATA_1                   | DATA_0 |
|-----------------------|-----------------------------|---------|-----------------------------------------|--------------------------|--------|
| master write access   | 0                           | 0x1004  | Offset                                  | ModuleEventChannelStatus |        |
| master read-          | 1                           | 0x1004  | Offset                                  |                          |        |
| HV board write access | 0                           | 0x1004  | Offset                                  | ModuleEventChannelStatus |        |
| Notes:                |                             |         |                                         |                          |        |
| Offset                | DATA_2Channel member offset |         | 0, 16, 32 ... access up to 255 channels |                          |        |
| EventChannelStatus    | DATA_0 to DATA_1            |         | UI2                                     |                          |        |

Table 124: module event channel status

### 3.5.2.10 ModuleEventChannelStatus32 (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR                    | DATA_ID | DATA_2 | DATA_3                                  | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|-----------------------------|---------|--------|-----------------------------------------|--------|--------|--------|
| master write access   | 0                           | 0x1084  | Offset | ModuleEventChannelStatus                |        |        |        |
| master read-          | 1                           | 0x1084  | Offset |                                         |        |        |        |
| HV board write access | 0                           | 0x1084  | Offset | ModuleEventChannelStatus                |        |        |        |
| Notes:                |                             |         |        |                                         |        |        |        |
| Offset                | DATA_2Channel member offset |         |        | 0, 16, 32 ... access up to 255 channels |        |        |        |
| EventChannelStatus32  | DATA_0 to DATA_3            |         |        | UI4                                     |        |        |        |

Table 125: module event channel status32

| Bit31 | Bit30 | Bit29 | Bit28 | Bit27 | Bit26 | Bit25 | Bit24 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CH31  | CH30  | Ch29  | CH28  | CH27  | CH26  | CH25  | CH24  |
| Bit23 | Bit22 | Bit21 | Bit20 | Bit19 | Bit18 | Bit17 | Bit16 |
| CH23  | CH22  | Ch21  | CH20  | CH19  | CH18  | CH17  | CH16  |
| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit09 | Bit08 |
| CH15  | CH14  | Ch13  | CH12  | CH11  | CH10  | CH9   | CH8   |
| Bit07 | Bit06 | Bit05 | Bit04 | Bit03 | Bit02 | Bit01 | Bit00 |
| CH07  | CH06  | CH05  | CH04  | CH03  | CH02  | CH01  | CH00  |

Table 126

The n-th bit of the register is set, if an event is active in the n-th channel and the associated bit in the EventMask register of the n-th channel is set too.

$$CHn = EventStatus[n] \& EventMask[n]$$

Reset of a bit is done by writing a 1 to this bit.

### 3.5.2.11 ModuleEventChannelMask (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR                    | DATA_ID | DATA_2                                  | DATA_1                 | DATA_0 |
|-----------------------|-----------------------------|---------|-----------------------------------------|------------------------|--------|
| master write access   | 0                           | 0x1005  | Offset                                  | ModuleEventChannelMask |        |
| master read-          | 1                           | 0x1005  | Offset                                  |                        |        |
| HV board write access | 0                           | 0x1005  | Offset                                  | ModuleEventChannelMask |        |
| Notes:                |                             |         |                                         |                        |        |
| Offset                | DATA_2Channel member offset |         | 0, 16, 32 ... access up to 255 channels |                        |        |
| EventChannelMask      | DATA_0 to DATA_1            |         | UI2                                     |                        |        |

Table 127

### 3.5.2.12 ModuleEventChannelMask32 (module write- / read-write access)

EDCP Frame:

| Access                | DATA_DIR                    | DATA_ID | DATA_2                                  | DATA_3                   | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|-----------------------------|---------|-----------------------------------------|--------------------------|--------|--------|--------|
| master write access   | 0                           | 0x1085  | Offset                                  | ModuleEventChannelMask32 |        |        |        |
| master read-          | 1                           | 0x1085  | Offset                                  |                          |        |        |        |
| HV board write access | 0                           | 0x1085  | Offset                                  | ModuleEventChannelMask32 |        |        |        |
| Notes:                |                             |         |                                         |                          |        |        |        |
| Offset                | DATA_2Channel member offset |         | 0, 16, 32 ... access up to 255 channels |                          |        |        |        |
| EventChannelMask32    | DATA_0 to DATA_3            |         | UI4                                     |                          |        |        |        |

Table 128

| Bit31     | Bit30     | Bit29     | Bit28     | Bit27     | Bit26     | Bit25     | Bit24     |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Mask CH31 | Mask CH30 | Mask CH29 | Mask CH28 | Mask CH27 | Mask CH26 | Mask CH25 | Mask CH24 |
| Bit23     | Bit22     | Bit21     | Bit20     | Bit19     | Bit18     | Bit17     | Bit16     |
| Mask CH23 | Mask CH22 | Mask CH21 | Mask CH20 | Mask CH19 | Mask CH18 | Mask CH17 | Mask CH16 |
| Bit15     | Bit14     | Bit13     | Bit12     | Bit11     | Bit10     | Bit09     | Bit08     |
| Mask CH15 | Mask CH14 | Mask CH13 | Mask CH12 | Mask CH11 | Mask CH10 | Mask CH9  | Mask CH8  |
| Bit07     | Bit06     | Bit05     | Bit04     | Bit03     | Bit02     | Bit01     | Bit00     |
| Mask CH7  | Mask CH6  | Mask CH5  | Mask CH4  | Mask CH3  | Mask CH2  | Mask CH1  | Mask CH0  |

Table 129

This register decides whether a pending event leads to the sum event flag of the module or not. If the n-th bit of the Mask is set and the n-th channel has an active event in the ModuleEventChannelStatus the bit isEventActive in the ModuleStatus register is set.

### 3.5.2.13 ModuleEventGroupStatus (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR         | DATA_ID | DATA_3                 | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|------------------|---------|------------------------|--------|--------|--------|
| master write access   | 0                | 0x1005  | ModuleEventGroupStatus |        |        |        |
| master read-          | 1                | 0x1005  |                        |        |        |        |
| HV board write access | 0                | 0x1005  | ModuleEventGroupStatus |        |        |        |
| Notes:                |                  |         |                        |        |        |        |
| EventGroupStatus      | DATA_0 to DATA_3 |         | UI4                    |        |        |        |

Table 130

| Bit31   | Bit30   | Bit29   | Bit28   | Bit27   | Bit26   | Bit25   | Bit24   |
|---------|---------|---------|---------|---------|---------|---------|---------|
| Group31 | Group30 | Group29 | Group28 | Group27 | Group26 | Group25 | Group24 |
| Bit23   | Bit22   | Bit21   | Bit20   | Bit19   | Bit18   | Bit17   | Bit16   |
| Group23 | Group22 | Group21 | Group20 | Group19 | Group18 | Group17 | Group16 |
| Bit15   | Bit14   | Bit13   | Bit12   | Bit11   | Bit10   | Bit09   | Bit08   |
| Group15 | Group14 | Group13 | Group12 | Group11 | Group10 | Group9  | Group8  |
| Bit07   | Bit06   | Bit05   | Bit04   | Bit03   | Bit02   | Bit01   | Bit00   |
| Group07 | Group06 | Group05 | Group04 | Group03 | Group02 | Group01 | Group00 |

Table 131

The n-th bit of this double word register is set, if an event is active in the n-th Group.

Reset of a bit is done by writing a 1 to this bit.

### 3.5.2.14 ModuleEventGroupMask (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR         | DATA_ID | DATA_3               | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|------------------|---------|----------------------|--------|--------|--------|
| master write access   | 0                | 0x1006  | ModuleEventGroupMask |        |        |        |
| master read-          | 1                | 0x1006  |                      |        |        |        |
| HV board write access | 0                | 0x1006  | ModuleEventGroupMask |        |        |        |
| Notes:                |                  |         |                      |        |        |        |
| EventGroupMask        | DATA_0 to DATA_3 |         | UI4                  |        |        |        |

Table 132

| Bit31  | Bit30  | Bit29  | Bit28  | Bit27  | Bit26  | Bit25  | Bit24  |
|--------|--------|--------|--------|--------|--------|--------|--------|
| Mask31 | Mask30 | Mask29 | Mask28 | Mask27 | Mask26 | Mask25 | Mask24 |
| Bit23  | Bit22  | Bit21  | Bit20  | Bit19  | Bit18  | Bit17  | Bit16  |
| Mask23 | Mask22 | Mask21 | Mask20 | Mask19 | Mask18 | Mask17 | Mask16 |
| Bit15  | Bit14  | Bit13  | Bit12  | Bit11  | Bit10  | Bit09  | Bit08  |
| Mask15 | Mask14 | Mask13 | Mask12 | Mask11 | Mask10 | Mask09 | Mask08 |
| Bit07  | Bit06  | Bit05  | Bit04  | Bit03  | Bit02  | Bit01  | Bit00  |
| Mask07 | Mask06 | Mask05 | Mask04 | Mask03 | Mask02 | Mask01 | Mask00 |

Table 133

This register decides whether a pending event leads to the sum event flag of the module or not. If the n-th bit of the mask is set and the n-th group has an active event in the ModuleEventGroupStatus the bit isEventActive in the ModuleStatus register is set.

### 3.5.2.15 VoltageRampSpeed (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR             | DATA_ID | DATA_3           | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------------------|---------|------------------|--------|--------|--------|
| master write access   | 0                    | 0x1100  | VoltageRampSpeed |        |        |        |
| master read-          | 1                    | 0x1100  |                  |        |        |        |
| HV board write access | 0                    | 0x1100  | VoltageRampSpeed |        |        |        |
| Notes:                |                      |         |                  |        |        |        |
| VoltageRampSpeed      | DATA_0 to DATA_3 [%] |         | R4               |        |        |        |

Table 134

|                                         |                                                                               |                                                                           |  |  |  |  |
|-----------------------------------------|-------------------------------------------------------------------------------|---------------------------------------------------------------------------|--|--|--|--|
| Voltage ramp speed range (disable Kill) | $1\text{mV/s} \leq \text{Ramp speed} \leq 20\% \text{ of } V_o \text{ max/s}$ |                                                                           |  |  |  |  |
| Option: fast ramp                       | 1                                                                             | $1\text{mV/s} \leq \text{Ramp speed} \leq 25\% \text{ of VoltageNominal}$ |  |  |  |  |
|                                         | 2                                                                             | $1\text{mV/s} \leq \text{Ramp speed} \leq 50\% \text{ of VoltageNominal}$ |  |  |  |  |
|                                         | 3                                                                             | $1\text{mV/s} \leq \text{Ramp speed} \leq 75\% \text{ of VoltageNominal}$ |  |  |  |  |

Voltage ramp speed range (enable Kill):  $1\text{mV/s} \leq \text{Ramp speed} \leq 1\% \text{ of } V_o \text{ max/s}$

The speed of the voltage ramp in percent of the nominal voltage of the channel per second.

### 3.5.2.16 CurrentRampSpeed – current controlled modules only (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR             | DATA_ID | DATA_3           | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------------------|---------|------------------|--------|--------|--------|
| master write access   | 0                    | 0x1101  | CurrentRampSpeed |        |        |        |
| master read-          | 1                    | 0x1101  |                  |        |        |        |
| HV board write access | 0                    | 0x1101  | CurrentRampSpeed |        |        |        |
| Notes:                |                      |         |                  |        |        |        |
| CurrentRampSpeed      | DATA_0 to DATA_3 [%] |         | R4               |        |        |        |

Table 135

Current ramp speed range:  $2\% \text{ IO max/s} \leq \text{Ramp speed} \leq \text{IO max/s}$

The speed of the current ramp in percent of the nominal current of the channel per second.

### 3.5.2.17 VoltageMax – OPTION (module read-write access)

EDCP frame:

| Access                | DATA_DIR             | DATA_ID | DATA_3     | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------------------|---------|------------|--------|--------|--------|
| master read-          | 1                    | 0x1102  |            |        |        |        |
| HV board write access | 0                    | 0x1102  | VoltageMax |        |        |        |
| Notes:                |                      |         |            |        |        |        |
| HardwareVoltageLimit  | DATA_0 to DATA_3 [%] |         | R4         |        |        |        |

Table 136

HV Modules with the OPTION hardware voltage limit can adjust VO max via the potentiometer Vmax.

For HV Modules without this OPTION VoltageMax equals to VO max.

The exceeding of the hardware voltage limit results in a limitation of the voltage when the KILL-enable.

The absolute value of the hardware voltage limit will compute by following:

$$\text{Voltage limit of the channel x (Chx)} = \text{VoltageNominal[Chx]} \cdot \text{VoltageMax}$$

The module responds after the hardware voltage limit has been exceeded:

The green LED on front panel is off.

Depends of the kind of module:

Hardware KILL function controlled by the bit 'KILena' of the ModuleControl word:

|                  |                                                                                                                                                               |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| KILL-enable = 1: | The voltage will be switched off permanently without ramp.<br>ChannelEventStatus flag 'EVLIM' will be set.                                                    |
| KILL-enable = 0: | The voltage will be reduced to the value of the actual hardware voltage limit.<br>ChannelStatus flag 'sVLIM' and ChannelEventStatus flag 'EVLIM' will be set. |

Software KILL function controlled by the bit 'KILena' of the ChannelControl word:

|                  |                                                                                                                                                                                                                               |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| KILL-enable = 1: | Voltage will be switched off permanently without ramp.<br>ChannelEventStatus flag 'EVLIM' will be set.                                                                                                                        |
| KILL-enable = 0: | Voltage will be switched off without ramp. If the output voltage arrives at 0 V the<br>ramping to set voltage will be restarted automatically. ChannelStatus flag 'sVLIM' and<br>ChannelEventStatus flag 'EVLIM' will be set. |

### 3.5.2.18 CurrentMax – OPTION (module read-write access)

EDCP frame:

| Access                | DATA_DIR             | DATA_ID | DATA_3     | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------------------|---------|------------|--------|--------|--------|
| master read-          | 1                    | 0x1103  |            |        |        |        |
| HV board write access | 0                    | 0x1103  | CurrentMax |        |        |        |
| Notes:                |                      |         |            |        |        |        |
| HardwareCurrentLimit  | DATA_0 to DATA_3 [%] |         | R4         |        |        |        |

Table 137

HV Modules with the OPTION CurrentMax can adjust the IO max via the potentiometer I<sub>max</sub>.

HV Modules without this OPTION deliver IO max.

The absolute value of the hardware current limit will compute by following:

$$\text{Current limit of the channel } x \text{ (Chx)} = \text{CurrentNominal[Chx]} \cdot \text{CurrentMax}$$

The module responds after the hardware current limit has been exceeded:

The green LED on front panel is off.

Depends of the kind of module:

Hardware KILL function controlled by the bit 'KILena' of the ModuleControl word:

KILL-enable = 1: Voltage will be switched off permanently without ramp. ChannelEventStatus flag 'ECLIM' will be set.

KILL-enable = 0: Current will be reduced to the value of the actual hardware current limit. ChannelStatus flag 'isCLIM' and ChannelEventStatus flag 'ECLIM' will be set.

Software KILL function controlled by the bit 'KILena' of the ChannelControl word:

KILL-enable = 1: Voltage will be switched off permanently without ramp. ChannelEventStatus flag 'ECLIM' will be set.

KILL-enable = 0: Voltage will be switched off without ramp. If the output voltage arrives at 0 V the ramping to set voltage will be restarted automatically. ChannelStatus flag 'isCLIM' and ChannelEventStatus flag 'ECLIM' will be set.

### 3.5.2.19 Supply24 (module read-write access)

EDCP frame:

| Access                | DATA_DIR             | DATA_ID | DATA_3   | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------------------|---------|----------|--------|--------|--------|
| master read-          | 1                    | 0x1104  |          |        |        |        |
| HV board write access | 0                    | 0x1104  | Supply24 |        |        |        |
| Notes:                |                      |         |          |        |        |        |
| Supply24              | DATA_0 to DATA_3 [V] |         | R4       |        |        |        |

Table 138

An 'out of range error' (see DCP group access: General status on page 98, in chapter 3.5.2.27 ADC SamplesPerSecond SPS (module write- / read-write access)) will be generated if deviation of voltage is more than  $\pm 10\%$ .

### 3.5.2.20 Supply5 (module read-write access)

EDCP frame:

| Access                | DATA_DIR | DATA_ID              | DATA_3  | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------|----------------------|---------|--------|--------|--------|
| master read-          | 1        | 0x1105               |         |        |        |        |
| HV board write access | 0        | 0x1105               | Supply5 |        |        |        |
| Notes:                |          |                      |         |        |        |        |
| Supply5               |          | DATA_0 to DATA_3 [V] | R4      |        |        |        |

Table 139

An 'out of range error' (see DCP group access: General status on page 98) will be generated if deviation of voltage is more than  $\pm 5\%$ .

### 3.5.2.21 BoardTemperature (module read-write access)

EDCP frame:

| Access                | DATA_DIR | DATA_ID               | DATA_3           | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------|-----------------------|------------------|--------|--------|--------|
| master read-          | 1        | 0x1106                |                  |        |        |        |
| HV board write access | 0        | 0x1106                | BoardTemperature |        |        |        |
| Notes:                |          |                       |                  |        |        |        |
| BoardTemperature      |          | DATA_0 to DATA_3 [°C] | R4               |        |        |        |

Table 140

An 'out of range error' (see group access: General status on page 98) will be generated if the temperature is higher than +55°C.

### 3.5.2.22 Threshold to arm the errors detection (module write / read- write access)

EDCP frame:

| Access                     | DATA_DIR | DATA_ID              | DATA_3                     | DATA_2 | DATA_1 | DATA_0 |
|----------------------------|----------|----------------------|----------------------------|--------|--------|--------|
| master write access        | 0        | 0x1107               | ThresholdArmErrorDetection |        |        |        |
| master read-               | 1        | 0x1107               |                            |        |        |        |
| HV board write access      | 0        | 0x1107               | ThresholdArmErrorDetection |        |        |        |
| Notes:                     |          |                      |                            |        |        |        |
| ThresholdArmErrorDetection |          | DATA_0 to DATA_3 [%] | R4                         |        |        |        |

Table 141

Factory setting for different kinds of HV modules is between 1V and to VO max/10 in percent to the nominal voltage of the channel.

The arming of the error detection is started while the actual voltage exceeds these value which has been stored before.

Exception: At the start of a ramp from zero the firmware evaluates that the feedback control will look in. If not, because the channel has a short or the hardware current limit is near to zero, then the channel will be switched off and a current error will be generated before the actual voltage is exceeding these threshold.

### 3.5.2.23 Serial number (module read-write access)

EDCP frame:

| Access                | DATA_DIR | DATA_ID          | DATA_3       | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------|------------------|--------------|--------|--------|--------|
| master read-          | 1        | 0x1200           |              |        |        |        |
| HV board write access | 0        | 0x1200           | SerialNumber |        |        |        |
| Notes:                |          |                  |              |        |        |        |
| SerialNumber          |          | DATA_0 to DATA_3 | UI4          |        |        |        |

Table 142

serial number e.g. 471212

### 3.5.2.24 Firmware release (module read-write access)

EDCP frame:

| Access                | DATA_DIR | DATA_ID          | DATA_3          | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------|------------------|-----------------|--------|--------|--------|
| master read-          | 1        | 0x1201           |                 |        |        |        |
| HV board write access | 0        | 0x1201           | FirmwareRelease |        |        |        |
| Notes:                |          |                  |                 |        |        |        |
| FirmwareRelease       |          | DATA_0 to DATA_3 | UI1[4]          |        |        |        |

Table 143

release e.g. 01.00.00.00

### 3.5.2.25 Bit rate (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR | DATA_ID                   | DATA_1  | DATA_0 |
|-----------------------|----------|---------------------------|---------|--------|
| master read-          | 1        | 0x1202                    |         |        |
| HV board write access | 0        | 0x1202                    | BitRate |        |
| Notes:                |          |                           |         |        |
| BitRate               |          | DATA_0 to DATA_1 [kbit/s] | UI2     |        |

Table 144

Following bit rates are possible: 20, 50, 100, 125, 250 kbit/s

The new bit rate gets active after RESET or POWER OFF/ON. The bit rate of all modules in the system must be the same before a RESET or POWER/ON is made.

- The bit rate is set to 250 kbit/s ex works.
- Invalid bit rates will be ignored and the bit 'Input error' of the will be set.
- A correct write access storing the information permanently if a NMT stop has been sent before.

### 3.5.2.26 Firmware Name (module read-write access)

EDCP frame:

| Access                | DATA_DIR                 | DATA_ID | DATA_4/5       | DATA_3 | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|--------------------------|---------|----------------|--------|--------|--------|--------|
| master write access   | 0                        | 0x1203  | NameOfFirmware |        |        |        |        |
| master read-          | 1                        | 0x1203  |                |        |        |        |        |
| HV board write access | 0                        | 0x1203  | NameOfFirmware |        |        |        |        |
| Notes:                |                          |         |                |        |        |        |        |
| NameOfFirmware        | DATA_0 to DATA_3 [ASCII] |         |                | BSTR   |        |        |        |

Table 145

| BSTR     | Description                                                                                                                         |
|----------|-------------------------------------------------------------------------------------------------------------------------------------|
| "E16D0"  | EDS 16 channel per board, distributor module, range of Vmax from VO max to (VO max - 1kV)                                           |
| "E16D1"  | EDS 16 channel per board, distributor module                                                                                        |
| "E08C0"  | EHS 8 channel per board, common GND module                                                                                          |
| "E08F0"  | EHS 8 channel per board, floating GND module                                                                                        |
| "E08F2"  | EHS 8 channel per board, floating GND module, two current measurement ranges                                                        |
| "E08F7"  | EHS STACK 8 channel per board, cascaded floating GND channels                                                                       |
| "E08C2"  | EHS 8 channel per board, common floating GND module, two current measurement ranges                                                 |
| "E16C1"  | EHS 16 channel per board or 32 channels per module, common GND module                                                               |
| "E24C1"  | EHS FLEX 24 channel per board or 48 channels per module, common GND module                                                          |
| "E24D1"  | EDS 24 channel per board, distributor module                                                                                        |
| "E24D3"  | EDS 24 channel per board, distributor module                                                                                        |
| "E04B0"  | EBS 4 channel per board, bipolar distributor module                                                                                 |
| "E08B0"  | EBS 8 channel per board, bipolar distributor module                                                                                 |
| "E12B0"  | EBS 12 channel per board, bipolar distributor module                                                                                |
| "N06C2"  | NHS NIM 6 channel module, common GND module, two current measurement ranges                                                         |
| "N04C2"  | NHR NIM 4 channel module, common GND module, two current measurement ranges, reversible voltages (currents), polarity is switchable |
| "MICC"   | MICC Multi channel Interface Crate Controller is a remote control interface for MMC Crates                                          |
| "MICP"   | MICP Multi channel Interface Crate PHQ Controller is a remote control interface for MMC Crates                                      |
| "H101C0" | HPS 19", 1 channel HV Power Supply (300W, 800W)                                                                                     |
| "H101C1" | HPS 19" 1 channel HV Power Supply 1.5kW - 10kW                                                                                      |
| "H201C0" | HPS compact 1channel HV Power Supply (350W)                                                                                         |

Table 146

### 3.5.2.27 ADC SamplesPerSecond SPS (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR               | DATA_ID | DATA_1                                                | DATA_0 |
|-----------------------|------------------------|---------|-------------------------------------------------------|--------|
| master write          | 0                      | 0x1204  | SamplesPerSecond                                      |        |
| Master read-          | 1                      | 0x1204  |                                                       |        |
| HV board write access | 0                      | 0x1204  | SamplesPerSecond                                      |        |
| Notes:                |                        |         |                                                       |        |
| SamplesPerSecond      | DATA_0 to DATA_1 [SPS] |         | UI2 (possible SPS are 500, 100, 60, 50, 25, 10 and 5) |        |

Table 147

Adjusts the number of averages of the programmable ADC filter of the HV modules. Possible values are 500, 100, 60 and 50 SPS. Notch should be set with 60 SPS using a 110V line with 60Hz and 50 SPS using a 230V line with 50Hz in order to improve the common-mode rejection of these frequencies. However a SPS value of the ADC will increase the main loop time by  $4 \cdot 1/\text{SPS}$  for devices "E08F0", "E08F2" (see page 97 chapter 3.5.2.26 Firmware Name (module read-write access)) respectively by  $4 \cdot 1/\text{SPS}$  multiplied with the number of channels for device "E16D0", "E08C0" (see page 97).

Factory settings:            E16D0, E08C0, E16C1, E08F0:            500 SPS  
                                      E08F2, E08C2:                        50 SPS.

### 3.5.2.28 DigitalFilter (module write- / read-write access)

EDCP frame:

| Access                | DATA_DIR                 | DATA_ID | DATA_1                                                | DATA_0 |
|-----------------------|--------------------------|---------|-------------------------------------------------------|--------|
| master write          | 0                        | 0x1205  | NumberOfSteps                                         |        |
| master read-          | 1                        | 0x1205  |                                                       |        |
| HV board write access | 0                        | 0x1205  | NumberOfSteps                                         |        |
| Notes:                |                          |         |                                                       |        |
| NumberOfSteps         | DATA_0 to DATA_1 [Steps] |         | UI2 (possible steps are 1, 16, 64, 256, 512 and 1024) |        |

Table 148

The digital filter in the firmware of the processor reduces the white noise of the analog values of channel VoltageMeasure, channel CurrentMeasure. The digital filtering gives the possibility to get a higher precision and to react fast on changes of the measured values. The filter is not used during a voltage ramp. The filter is restarted after a significant change of the signal.

Factory settings:    64

### 3.5.2.29 ChannelNumber (module read access)

EDCP frame:

| Access                | DATA_DIR         | DATA_ID | DATA_3        | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|------------------|---------|---------------|--------|--------|--------|
| master read-          | 1                | 0x1208  |               |        |        |        |
| HV board write access | 0                | 0x1208  | ChannelNumber |        |        |        |
| Notes:                |                  |         |               |        |        |        |
| ChannelNumber         | DATA_0 to DATA_3 |         | UI4           |        |        |        |

Table 149

### 3.5.2.30 ArticleDescription (module read access)

EDCP frame:

| Access                | DATA_DIR         | DATA_ID | DATA_5             | DATA_4 | DATA_3 | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|------------------|---------|--------------------|--------|--------|--------|--------|--------|
| master read-          | 1                | 0x1209  |                    |        |        |        |        |        |
| HV board write access | 0                | 0x1209  | ArticleDescription |        |        |        |        |        |
| Notes:                |                  |         |                    |        |        |        |        |        |
| ArticleDescription    | DATA_0 to DATA_3 |         |                    | UI4    |        |        |        |        |

Table 150

This register returns the module article description. Depending on the length of the article description, multiple CAN messages may be sent. The description is terminated by a zero character.

### 3.5.2.31 ModuleOption (module read access)

EDCP frame:

| Access                | DATA_DIR         | DATA_ID | DATA_3       | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|------------------|---------|--------------|--------|--------|--------|
| master read-          | 1                | 0x1280  |              |        |        |        |
| HV board write access | 0                | 0x1280  | ModuleOption |        |        |        |
| Notes:                |                  |         |              |        |        |        |
| ModuleOption          | DATA_0 to DATA_3 |         | UI4          |        |        |        |

The requested value of the module option is not valid when all bits are set to '1'!

| Bit31    | Bit30    | Bit29     | Bit28              | Bit27             | Bit26           | Bit25        | Bit24           |
|----------|----------|-----------|--------------------|-------------------|-----------------|--------------|-----------------|
| EDCP     | Reserved | Reserved  | Reserved           | Reserved          | HVBPM           | CLIM         | VLIM            |
| Bit23    | Bit22    | Bit21     | Bit20              | Bit19             | Bit18           | Bit17        | Bit16           |
| INHIBIT  | RELAY    | FAST RAMP | SAFETY LOOP ACTIVE | BLOCK KILL ENABLE | BLOCK EMERGENCY | INHIBIT DOWN | INHIBIT NEGATED |
| Bit15    | Bit14    | Bit13     | Bit12              | Bit11             | Bit10           | Bit09        | Bit08           |
| Reserved | Reserved | Reserved  | Reserved           | Reserved          | Reserved        | Reserved     | Reserved        |
| Bit07    | Bit06    | Bit05     | Bit04              | Bit03             | Bit02           | Bit01        | Bit00           |
| Reserved | IEEE 488 | PLC       | AIO                | USB               | ETH             | RS232        | CAN             |

Table 151

| BIT   | OPTION             | DESCRIPTION /SPECIFICATION                                                                                                                 |
|-------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| Bit31 | EDCP               | Device use the iseg Enhanced Device Control Protocol                                                                                       |
| Bit26 | HVBM               | HV boards per (CAN nodes) module                                                                                                           |
| Bit25 | CLIM               | hardware current limit                                                                                                                     |
| Bit24 | VLIM               | hardware voltage limit                                                                                                                     |
| Bit23 | INHIBIT            | external INHIBIT signals will be monitored, option IU, ID, NIU and NID in combination with Bit17, INHIBIT DOWN and bit 16, INHIBIT INVERSE |
| Bit22 | RELAY              | discharge relay                                                                                                                            |
| Bit21 | FAST RAMP          | fast ramp                                                                                                                                  |
| Bit20 | SAFETY LOOP ACTIVE | Opened the safety loop active by the module, option SLA                                                                                    |
| Bit19 | BLOCK KILL ENABLE  | Blocked any try to set kill enable bit                                                                                                     |
| Bit18 | BLOCK EMERGENCY    | Blocked any try to switch on the emergency bit                                                                                             |
| Bit17 | INHIBIT DOWN       | Configure pull down resistors on the inhibit inputs lines                                                                                  |
| Bit16 | INHIBIT NEGATED    | Negate handling of the INHIBIT signals                                                                                                     |
| Bit06 | IEEE 488           | Implements an IEEE 488 compatible interface                                                                                                |
| Bit05 | PLC                | Implements an interface to connect a PLC (Programmable Logic Control)                                                                      |
| Bit04 | AIO                | Implements an Analog I/O interface                                                                                                         |
| Bit03 | USB                | Implements an USB interface                                                                                                                |
| Bit02 | ETH                | Implements an Ethernet interface                                                                                                           |
| Bit01 | RS232              | Implements a RS232 interface                                                                                                               |
| Bit00 | CAN                | Implements a CAN interface                                                                                                                 |

Table 152

### 3.5.2.32 ModuleOptionSpec (module read access)

EDCP frame:

| Access                | DATA_DIR         | DATA_ID | DATA_4       | DATA_3 | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|------------------|---------|--------------|--------|--------|--------|--------|
| master read-          | 1                | 0x1290  | DATA_4       | DATA_3 | DATA_2 | DATA_1 |        |
| HV board write access | 0                | 0x1290  | ModuleOption |        |        |        | Spec   |
| Notes:                |                  |         |              |        |        |        |        |
| ModuleOption          | DATA_1 to DATA_4 |         |              | UI4    |        |        |        |
| Specfication          | DATA_0           |         |              | UI1    |        |        |        |

Table 153

The requested value of the module option specification is not valid or do not exist when all bits are set to '1' or '0'!

| Bit31                            | Bit30 | Bit29     | Bit28 | Bit27 | Bit26                            | Bit25         | Bit24         |
|----------------------------------|-------|-----------|-------|-------|----------------------------------|---------------|---------------|
| Enhanced Device Control Protocol | –     | –         | –     | –     | HV boards per (CAN nodes) module | Current limit | Voltage limit |
| Bit23                            | Bit22 | Bit21     | Bit20 | Bit19 | Bit18                            | Bit17         | Bit16         |
| INHIBIT                          | RELAY | Fast RAMP | –     | –     | –                                | –             | –             |
| Bit15                            | Bit14 | Bit13     | Bit12 | Bit11 | Bit10                            | Bit09         | Bit08         |
| –                                | –     | –         | –     | –     | –                                | –             | –             |
| Bit07                            | Bit06 | Bit05     | Bit04 | Bit03 | Bit02                            | Bit01         | Bit00         |
| –                                | –     | –         | –     | –     | –                                | –             | –             |

Table 154

To request a specification the corresponding bit of the module option word has to be set to '1'.

|                |           |   |                       |
|----------------|-----------|---|-----------------------|
| Specification: | fast ramp | 1 | 25% of VoltageNominal |
|                |           | 2 | 50% of VoltageNominal |
|                |           | 3 | 75% of VoltageNominal |

### 3.5.2.33 ModuleCommMode (module write access)

EDCP frame:

| Access                | DATA_DIR         | DATA_ID | DATA_1         | DATA_0 |
|-----------------------|------------------|---------|----------------|--------|
| HV board write access | 0                | 0x12a0  | ModuleCommMode |        |
| Notes:                |                  |         |                |        |
| ModuleOption          | DATA_0 to DATA_3 |         | UI2            |        |

Table 155

| Bit31    | Bit30    | Bit29    | Bit28    | Bit27    | Bit26    | Bit25    | Bit24    |
|----------|----------|----------|----------|----------|----------|----------|----------|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Bit23    | Bit22    | Bit21    | Bit20    | Bit19    | Bit18    | Bit17    | Bit16    |
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Bit15    | Bit14    | Bit13    | Bit12    | Bit11    | Bit10    | Bit09    | Bit08    |
| –        | –        | –        | –        | –        | –        | –        | –        |
| Bit07    | Bit06    | Bit05    | Bit04    | Bit03    | Bit02    | Bit01    | Bit00    |
| –        | –        | –        | –        | –        | –        | –        | FAST     |

Table 156

| Bit  | Level | Description |
|------|-------|-------------|
| Bit0 | FAST  | 1           |
|      |       | 0           |
|      |       | common mode |

Table 157

### 3.5.3 EDCP Group Accesses

The Multi Channel CAN module offers an extended and flexible range of group functions. There exist both predefined (so called fix) groups and variable groups.

Each group definition consists of 2 words each of 16 bits. In fix groups these 2 words are the value to be set into all channels (in float format) or they are a logical information. In variable groups one word carries the information about type and characteristics of the group, the other word carries the information about the members of the group or gives an overview about a selected situation in all channels.

Four different group types for variable groups have been established:

- Set group
- Status group
- Monitoring group
- Trip group

### 3.5.3.1 SetGroup

Set groups will be used in order to set channels to a same value, which happen to carry the identical channel value. Therefore within the group following will be defined:

- Member of the group: Channel members acts for the control set bit of the master channel.
- Type of the group: Set group type TypeSet.
- Channel characteristics: Coding of characteristics, which have to be set commonly.
- Control mode: Divides between a one-time setting of the slave channel property and a permanently copying of the Master channel's property to the slave channels.
- Master channel: Number of the channel, which characteristics will be transferred to the other channels. Is just necessary for Set groups which set a value.  
If functions have to be initialized e.g. start of ramp then there is no Master channel.

#### EDCP frame:

| Access                | DATA_DIR                | DATA_ID | NBR                                         | OFFSET | DATA_5     | DATA_2  | DATA_1 | DATA_0 |
|-----------------------|-------------------------|---------|---------------------------------------------|--------|------------|---------|--------|--------|
| master group write    | 0                       | 0x2000  | Nx                                          | Ox     | MembersSet | TypeSet |        |        |
| master group read-    | 1                       | 0x2000  | Nx                                          | Ox     |            |         |        |        |
| HV board write access | 0                       | 0x2000  | Nx                                          | Ox     | MembersSet | TypeSet |        |        |
| Notes:                |                         |         |                                             |        |            |         |        |        |
| Nx                    | Group number            |         | 0 ... 31                                    |        |            | UI1     |        |        |
| Ox                    | Channel member offset   |         | 0, 16, 32 ... too access up to 255 channels |        |            | UI1     |        |        |
| MembersSet            | Channel members setting |         | members 0x000001 ... 0xFFFFF                |        |            | UI4     |        |        |
| TypeSet               | Setting type            |         |                                             |        |            | UI2     |        |        |

Table 158

#### MembersSet:

| Bit31    | Bit30    | Bit29    | Bit28    | Bit27    | Bit26    | Bit25    | Bit24    |
|----------|----------|----------|----------|----------|----------|----------|----------|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Bit23    | Bit22    | Bit21    | Bit20    | Bit19    | Bit18    | Bit17    | Bit16    |
| CH23     | CH22     | CH21     | CH20     | CH19     | CH18     | CH17     | CH16     |
| Bit15    | Bit14    | Bit13    | Bit12    | Bit11    | Bit10    | Bit09    | Bit08    |
| CH15     | CH14     | CH13     | CH12     | CH11     | CH10     | CH9      | CH8      |
| Bit07    | Bit06    | Bit05    | Bit04    | Bit03    | Bit02    | Bit01    | Bit00    |
| CH7      | CH6      | CH5      | CH4      | CH3      | CH2      | CH1      | CH0      |

Table 159

**TypeSet:**

| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit09 | Bit08 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TYPE1 | TYPE0 | res   | res   | res   | res   | res   | MOD0  |
| Bit07 | Bit06 | Bit05 | Bit04 | Bit03 | Bit02 | Bit01 | Bit00 |
| SET3  | SET2  | SET1  | SET0  | MCH3  | MCH2  | MCH1  | MCH0  |

Table 160

**Channel members:**

| MembersSet          | Value                |                                                                                                                                                                              |
|---------------------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CH23, CH22, ... CH0 | 0x000001 ... 0xFFFFF | The HV channels which can be configured here as members will follow a setting type defined by the bits SET0 to SET3 for the master channel defined by the bits MCH0 to MCH3. |

Table 161

**Group type:**

| TYPE1 | TYPE0 | Value        |                               |
|-------|-------|--------------|-------------------------------|
| 0     | 0     | SetGroupType | Group is defined as Set group |

Table 162

**Mode:**

| MOD0 | Value |                                        |
|------|-------|----------------------------------------|
| 0    | 0     | The group function is done one time    |
| 1    | 1     | The group function is done permanently |

Table 163

**Setting type:**

| SET3 | SET2 | SET1 | SET0 | Value         |                                                                    |
|------|------|------|------|---------------|--------------------------------------------------------------------|
| 0    | 0    | 0    | 1    | SetVset       | Copy Vset from MCH to all members                                  |
| 0    | 0    | 1    | 0    | SetIset       | Copy Iset from MCH to all members                                  |
| 0    | 1    | 0    | 0    | SetVbnds      | Copy Vbounds from MCH to all members                               |
| 0    | 1    | 0    | 1    | SetIbnds      | Copy Ibounds from MCH to all members                               |
| 1    | 0    | 1    | 0    | SetOn         | Switch ON/OFF all members depending on setON in MCH                |
| 1    | 0    | 1    | 1    | SetEmrgCutOff | Switch OFF all members (Emergency OFF)                             |
| 1    | 1    | 1    | 1    | Cloning       | Set all properties of members like MCH properties (in preparation) |

Table 164

#### Master channel:

| MCH3 | MCH2 | MCH1 | MCH0 | Value |                                     |
|------|------|------|------|-------|-------------------------------------|
| 0    | 0    | 0    | 0    | 0     | 1: Channel 0 is MasterChannel MCH   |
| 0    | 0    | 0    | 1    | 1     | 1: Channel 1 is MasterChannel MCH   |
| ...  | ...  | ...  | ...  | ...   | ...                                 |
| 1    | 1    | 1    | 1    | 15    | 1: Channel 15 ist MasterChannel MCH |

Table 165

#### 3.5.3.2 StatusGroup

Status groups are used to report the status of a single characteristic of all channels simultaneously. No action is foreseen.

Therefore within the group following has to be defined:

- Members of the group: Channel members of a specific channel status bit
- Type of the group: Status group type TypeStatus
- Channel characteristics: Coding of characteristics which is to be reported.

#### EDCP frame:

| Access                | DATA_DIR | DATA_ID                | NBR                                         | OFFSET | DATA_5        | DATA_2 | DATA_1     | DATA_0 |
|-----------------------|----------|------------------------|---------------------------------------------|--------|---------------|--------|------------|--------|
| master group write    | 0        | 0x2000                 | Nx                                          | Ox     | MembersStatus |        | TypeStatus |        |
| master group read-    | 1        | 0x2000                 | Nx                                          | Ox     |               |        |            |        |
| HV board write access | 0        | 0x2000                 | Nx                                          | Ox     | MembersStatus |        | TypeStatus |        |
| Notes:                |          |                        |                                             |        |               |        |            |        |
| Nx                    |          | Group number           | 0 ... 31                                    |        |               |        | UI1        |        |
| Ox                    |          | Channel member offset  | 0, 16, 32 ... too access up to 255 channels |        |               |        | UI1        |        |
| MembersStatus         |          | Channel members status | members 0x000000 ... 0xFFFFF                |        |               |        | UI4        |        |
| TypeStatus            |          | Status type            |                                             |        |               |        | UI2        |        |

Table 166

#### MemberStatus:

| Bit31    | Bit30    | Bit29    | Bit28    | Bit27    | Bit26    | Bit25    | Bit24    |
|----------|----------|----------|----------|----------|----------|----------|----------|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Bit23    | Bit22    | Bit21    | Bit20    | Bit19    | Bit18    | Bit17    | Bit16    |
| CH23     | CH22     | CH21     | CH20     | CH19     | CH18     | CH17     | CH16     |
| Bit15    | Bit14    | Bit13    | Bit12    | Bit11    | Bit10    | Bit09    | Bit08    |
| CH15     | CH14     | CH13     | CH12     | CH11     | CH10     | CH9      | CH8      |
| Bit07    | Bit06    | Bit05    | Bit04    | Bit03    | Bit02    | Bit01    | Bit00    |
| CH7      | CH6      | CH5      | CH4      | CH3      | CH2      | CH1      | CH0      |

Table 167

**TypeStatus:**

| Bit15 | Bit14 | Bit13    | Bit12    | Bit11    | Bit10    | Bit09    | Bit08    |
|-------|-------|----------|----------|----------|----------|----------|----------|
| TYPE1 | TYPE0 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Bit07 | Bit06 | Bit05    | Bit04    | Bit03    | Bit02    | Bit01    | Bit00    |
| STAT3 | STAT2 | STAT1    | STAT0    | Reserved | Reserved | Reserved | Reserved |

Table 168

**Channel members:**

| MembersStatus       | Value                   |                                                                                                                                    |
|---------------------|-------------------------|------------------------------------------------------------------------------------------------------------------------------------|
| CH23, CH22, ... CH0 | 0x000000 ... 0xFFFFFFFF | Combine HV channels which are in status defined by the bits SET[3 ... 0] for the master channel defined by the bits MCH0[3 ... 0]. |

Table 169

**Group type:**

| TYPE1 | TYPE0 | Value           |                                       |
|-------|-------|-----------------|---------------------------------------|
| 0     | 1     | StatusGroupType | Group will be defined as Status group |

Table 170

**Status type:**

| STAT3 | STAT2 | STAT1 | STAT0 | Value                |                                                         |
|-------|-------|-------|-------|----------------------|---------------------------------------------------------|
| 0     | 0     | 1     | 1     | ChkIsOn              | check channel Status.isON (is on)                       |
| 0     | 1     | 0     | 0     | ChkIsRamping         | check channel Status.isRAMP (is ramping)                |
| 0     | 1     | 1     | 0     | ChkIsConstantCurrent | check channel Status.isCC (is current control)          |
| 0     | 1     | 1     | 1     | ChkIsConstantVoltage | check channel Status.isCV (is voltage control)          |
| 1     | 0     | 1     | 0     | ChkIsCurrentBounds   | check channel Status.isCBNDs (is current bounds)        |
| 1     | 0     | 1     | 1     | ChkIsVoltageBounds   | check channel Status.isVBNDs (is voltage bounds)        |
| 1     | 1     | 0     | 0     | ChkIsExternalInhibit | check channel Status.isEINH (is external inhibit)       |
| 1     | 1     | 0     | 1     | ChkIsTrip            | check channel Status.isTRIP (is trip)                   |
| 1     | 1     | 1     | 0     | ChkIsCurrentLimit    | check channel Status.isCLIM (is current limit exceeded) |
| 1     | 1     | 1     | 1     | ChkIsVoltageLimit    | check channel Status.isVLIM (is voltage limit exceeded) |

Table 171

### 3.5.3.3 MonitoringGroup

Monitoring groups are used to observe a single characteristic of selected channels simultaneously and in case of need take action. Therefore the group has to be defined:

- Members of the group: Channel members acts for the configured status monitor bit.
- Type of the group: Monitoring group type TypeMon
- Channel characteristics: Coding of characteristics which is to be monitored.
- Control mode: Coding of the control function, i.e. which kind of change in the group-image shall cause a signal.
- Activity: Define which activity has to happen after the event.

#### EDCP frame:

| Access                | DATA_DIR                   | DATA_ID | NBR                                         | OFFSET | DATA_5            | DATA_2         | DATA_1 | DATA_0 |
|-----------------------|----------------------------|---------|---------------------------------------------|--------|-------------------|----------------|--------|--------|
| master group write    | 0                          | 0x2000  | Nx                                          | Ox     | MembersMonitoring | TypeMonitoring |        |        |
| master group read-    | 1                          | 0x2000  | Nx                                          | Ox     |                   |                |        |        |
| HV board write access | 0                          | 0x2000  | Nx                                          | Ox     | MembersMonitoring | TypeMonitoring |        |        |
| Notes:                |                            |         |                                             |        |                   |                |        |        |
| Nx                    | Group number               |         | 0 ... 31                                    |        |                   |                | UI1    |        |
| Ox                    | Channel member offset      |         | 0, 16, 32 ... too access up to 255 channels |        |                   |                | UI1    |        |
| MembersMonitoring     | Channel monitoring members |         | 0x000001 ... 0xFFFFF                        |        |                   |                | UI4    |        |
| TypeMonitoring        | Monitoring type            |         |                                             |        |                   |                | UI2    |        |

Table 172

#### ChannelMonitoringList:

| Bit31    | Bit30    | Bit29    | Bit28    | Bit27    | Bit26    | Bit25    | Bit24    |
|----------|----------|----------|----------|----------|----------|----------|----------|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Bit23    | Bit22    | Bit21    | Bit20    | Bit19    | Bit18    | Bit17    | Bit16    |
| CH23     | CH22     | CH21     | CH20     | CH19     | CH18     | CH17     | CH16     |
| Bit15    | Bit14    | Bit13    | Bit12    | Bit11    | Bit10    | Bit09    | Bit08    |
| CH15     | CH14     | CH13     | CH12     | CH11     | CH10     | CH9      | CH8      |
| Bit07    | Bit06    | Bit05    | Bit04    | Bit03    | Bit02    | Bit01    | Bit00    |
| CH7      | CH6      | CH5      | CH4      | CH3      | CH2      | CH1      | CH0      |

Table 173

**TypeMonitoring:**

| Bit15 | Bit14 | Bit13 | Bit12 | Bit11    | Bit10    | Bit09    | Bit08    |
|-------|-------|-------|-------|----------|----------|----------|----------|
| TYPE1 | TYPE0 | ACT1  | ACT0  | res      | res      | res      | MOD0     |
| Bit07 | Bit06 | Bit05 | Bit04 | Bit03    | Bit02    | Bit01    | Bit00    |
| MON3  | MON2  | MON1  | MON0  | Reserved | Reserved | Reserved | Reserved |

Table 174

**Channel members:**

| MembersMonitoring   | Value                |                                                                                                                                              |
|---------------------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| CH23, CH22, ... CH0 | 0x000000 ... 0xFFFFF | Combine HV channels which monitor the status bits configured in bit MON[3 ... 0] and acts to the action configured by the bits ACT[1 ... 0]. |

Table 175

**Group type:**

| TYPE1 | TYPE0 | Value               | Description                               |
|-------|-------|---------------------|-------------------------------------------|
| 1     | 0     | MonitoringGroupType | Group will be defined as Monitoring group |

Table 176

**Monitoring action:**

| ACT1 | ACT0 | Value | Description                                                      |
|------|------|-------|------------------------------------------------------------------|
| 0    | 0    | 0     | No special action ; EventGroupStatus[grp] will be set            |
| 0    | 1    | 1     | Ramp down of group EventGroupStatus[grp] will be set             |
| 1    | 0    | 2     | Shut down group without ramp; EventGroupStatus[grp] will be set  |
| 1    | 1    | 3     | Shut down module without ramp; EventGroupStatus[grp] will be set |

Table 177

**Mode:**

| MOD0 | Value | Description                                    |
|------|-------|------------------------------------------------|
| 0    | 0     | event will happen if at least one Channel == 0 |
| 1    | 1     | event will happen if at least one Channel == 1 |

Table 178

**Monitor type:**

| MON3 | MON2 | MON1 | MON0 | Value                    | Description                                                |
|------|------|------|------|--------------------------|------------------------------------------------------------|
| 0    | 0    | 1    | 1    | MonitorIsOn              | monitor channel Status.isON (is on)                        |
| 0    | 1    | 0    | 0    | MonitorIsRamping         | monitor channel Status.isRAMP (is ramping)                 |
| 0    | 1    | 1    | 0    | MonitorIsConstantCurrent | monitor channel Status.isCC (is Constant Current)          |
| 0    | 1    | 1    | 1    | MonitorIsConstantVoltage | monitor channel Status.isCV (is Constant Voltage)          |
| 1    | 0    | 1    | 0    | MonitorIsCurrentBounds   | monitor channel Status.isCBNDs (is Current Bounds)         |
| 1    | 0    | 1    | 1    | MonitorIsVoltageBounds   | monitor channel Status.isVBNDs (is Voltage Bounds)         |
| 1    | 1    | 0    | 0    | MonitorIsExternalInhibit | monitor channel Status.isEINH (is External Inhibit)        |
| 1    | 1    | 0    | 1    | MonitorIsTrip            | monitor channel Status.isTRIP (is Trip)                    |
| 1    | 1    | 1    | 0    | MonitorIsCurrentLimit    | monitor channel Status.isCLIM (is Current Limit exceeded.) |
| 1    | 1    | 1    | 1    | MonitorIsVoltageLimit    | monitor channel Status.isVLIM (is Voltage Limit exceeded.) |

Table 179

### 3.5.3.4 DelayedTripGroup

Trip timeout groups are necessary to keep the timing for the time controlled delayed Trip function and to define the action which has to happen after a Trip.

Therefore in the group following will be defined:

- Members of the group: Channel members acts to the configured action when constant current state is active longer than the trip time out is configured.
- Type of the group: Group time out type
- Activity: Define which activity has to happen after time controlled Trip
- Timeout: Coding of Timeout-time as integer value.

Timeout groups have to stay unchanged for the whole time as long they are used.

An overwriting will cause the definition of a new group. An overlay of the channels of multiple Trip groups is not allowed.

#### EDCP frame:

| Access                | DATA_DIR                     | DATA_ID | NBR | OFFSET                                      | DATA_5             | DATA_2 | DATA_1       | DATA_0 |
|-----------------------|------------------------------|---------|-----|---------------------------------------------|--------------------|--------|--------------|--------|
| master group write    | 0                            | 0x2000  | Nx  | Ox                                          | MembersTripTimeout |        | TypeTripTime |        |
| master group read-    | 1                            | 0x2000  | Nx  | Ox                                          |                    |        |              |        |
| HV board write access | 0                            | 0x2000  | Nx  | Ox                                          | MembersTripTimeout |        | TypeTripTime |        |
| Notes:                |                              |         |     |                                             |                    |        |              |        |
| Nx                    | Group number                 |         |     | 0 ... 31                                    |                    |        | UI1          |        |
| Ox                    | Channel member offset        |         |     | 0, 16, 32 ... too access up to 255 channels |                    |        | UI1          |        |
| MembersTripTimeout    | Channel trip timeout members |         |     | 0x000001 ... 0xFFFFFFFF                     |                    |        | UI4          |        |
| TypeTime              | Type time out                |         |     |                                             |                    |        | UI2          |        |

Table 180: EDCP

#### MembersTripTimeout:

| Bit31    | Bit30    | Bit29    | Bit28    | Bit27    | Bit26    | Bit25    | Bit24    |
|----------|----------|----------|----------|----------|----------|----------|----------|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| Bit23    | Bit22    | Bit21    | Bit20    | Bit19    | Bit18    | Bit17    | Bit16    |
| CH23     | CH22     | CH21     | CH20     | CH19     | CH18     | CH17     | CH16     |
| Bit15    | Bit14    | Bit13    | Bit12    | Bit11    | Bit10    | Bit09    | Bit08    |
| CH15     | CH14     | CH13     | CH12     | CH11     | CH10     | CH9      | CH8      |
| Bit07    | Bit06    | Bit05    | Bit04    | Bit03    | Bit02    | Bit01    | Bit00    |
| CH7      | CH6      | CH5      | CH4      | CH3      | CH2      | CH1      | CH0      |

Table 181: Members Trip Timeout

**TypeTripTime:**

| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit09 | Bit08 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TYPE1 | TYPE0 | ACT1  | ACT0  | TOT11 | TOT10 | TOT9  | TOT8  |
| Bit07 | Bit06 | Bit05 | Bit04 | Bit03 | Bit02 | Bit01 | Bit00 |
| TOT7  | TOT6  | TOT5  | TOT4  | TOT3  | TOT2  | TOT1  | TOT0  |

Table 182

**Channel members:**

| MembersMonitoring   | Value                                                                                                                                                                 |
|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CH23, CH22, ... CH0 | 0x000000 ... 0xFFFFF<br>The configured HV channels will be tripped when one of it is in status constant current longer than the time out configured in TOT[11 ... 0]. |

Table 183: Channel members

**Group type:**

| TYPE1 | TYPE0 | Value                                                      |
|-------|-------|------------------------------------------------------------|
| 1     | 1     | TimeOutGroupType<br>Group will be defined as Timeout group |

Table 184: Group type

**Trip timeout action:**

| ACT1 | ACT0 | Action                                                                    |
|------|------|---------------------------------------------------------------------------|
| 0    | 0    | 0<br>No special action; EventGroupStatus[grp] will be set.                |
| 0    | 1    | 1<br>Ramp down group with ramp; EventGroupStatus[grp] will be set         |
| 1    | 0    | 2<br>Shut down the group without ramp; EventGroupStatus[grp] will be set  |
| 1    | 1    | 3<br>Shut down the module without ramp; EventGroupStatus[grp] will be set |

Table 185: Trip timeout action

| INFORMATION                                                                                        |                                                                                                             |
|----------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|
| <br>INFORMATION | TOT[11 ... 0]:                                                                                              |
|                                                                                                    | Timeout-time in ms (8 ... 4088 ms) resolution is 8 ms (different values to 8 ms resolution will be rounded) |

### 3.5.3.5 Request Temperatures and Supplies (group write access)

| Message                       | DLC | DataID | Channel | Data | Data | Data | Data | Value   |
|-------------------------------|-----|--------|---------|------|------|------|------|---------|
| Request all Temperatures      | 2   | 20 01  |         |      |      |      |      |         |
| Temperature 0                 | 7   | 20 01  | 00      | 41   | EF   | 0D   | B0   | 29.9 °C |
| Temperature 1                 | 7   | 20 01  | 01      | 41   | ED   | 66   | 30   | 29.7 °C |
| Temperature 2                 | 7   | 20 01  | 02      | 41   | EF   | 0D   | B0   | 29.9 °C |
| Request all Measured Supplies | 2   | 20 02  |         |      |      |      |      |         |
| Positive supply external +24  | 7   | 20 02  | 00      | 41   | BE   | 75   | 98   | 23,8 V  |
| Negative supply external -24  | 7   | 20 02  | 01      | C1   | C0   | 00   | 00   | -24 V   |
| Logic supply external +5      | 7   | 20 02  | 02      | 40   | A0   | 51   | EC   | 5,01 V  |
| Positive supply op-amp        | 7   | 20 02  | 03      | 41   | 40   | 00   | 00   | 12      |
| Negative supply op-amp        | 7   | 20 02  | 04      | C1   | 40   | 00   | 00   | -12     |
| Logic intern +5               | 7   | 20 02  | 05      | 40   | A0   | 51   | EC   | 4.99 V  |
| Ligic intern +3.3             | 7   | 20 02  | 06      | 40   | 53   | 2E   | 1C   | 3.29 V  |
| Reserved                      | 7   | 20 02  | 07      | 00   | 00   | 00   | 00   | 0 (res) |
| Reserved                      | 7   | 20 02  | 08      | 00   | 00   | 00   | 00   | 0 (res) |

Table 186: Request Temperatures and Supplies

### 3.5.3.6 GroupVoltageLimit – OPTION (module read-write access)

EDCP frame:

| Access                | DATA_DIR | DATA_ID              | DATA_4  | DATA_3     | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------|----------------------|---------|------------|--------|--------|--------|
| master read -         | 1        | 0x2005               |         |            |        |        |        |
| HV board write access | 0        | 0x2005               | Channel | VoltageMax |        |        |        |
| Notes:                |          |                      |         |            |        |        |        |
| HardwareVoltageLimit  |          | DATA_0 to DATA_3 [%] |         | R4         |        |        |        |
| VoltageMax            |          |                      |         |            |        |        |        |
| Channel               |          |                      |         |            |        |        |        |

Table 187

### 3.5.3.7 GroupCurrentLimit – OPTION (module read-write access)

EDCP frame:

| Access                | DATA_DIR | DATA_ID              | DATA_4  | DATA_3     | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------|----------------------|---------|------------|--------|--------|--------|
| master read -         | 1        | 0x2006               |         |            |        |        |        |
| HV board write access | 0        | 0x2006               | Channel | CurrentMax |        |        |        |
| Notes:                |          |                      |         |            |        |        |        |
| HardwareVoltageLimit  |          | DATA_0 to DATA_3 [%] |         | R4         |        |        |        |
| CurrentMax            |          |                      |         |            |        |        |        |
| Channel               |          |                      |         |            |        |        |        |

Table 188

### 3.5.3.8 VoltageSetAllChannels (group write access)

EDCP frame:

| Access                | DATA_DIR             | DATA_ID | DATA_3                | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------------------|---------|-----------------------|--------|--------|--------|
| master write access   | 0                    | 0x2100  | VoltageSetAllChannels |        |        |        |
| Notes:                |                      |         |                       |        |        |        |
| VoltageSetAllChannels | DATA_0 to DATA_3 [A] |         | R4                    |        |        |        |

Table 189

(see 3.5.1.14 Set current / trip (single write- and single/ multiple single read-write access) Single access also)

### 3.5.3.9 Current-Trip/Set-AllChannels (group write access)

EDCP frame:

| Access                | DATA_DIR             | DATA_ID | DATA_3                | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|----------------------|---------|-----------------------|--------|--------|--------|
| master write access   | 0                    | 0x2101  | CurrentSetAllChannels |        |        |        |
| Notes:                |                      |         |                       |        |        |        |
| CurrentSetAllChannels | DATA_0 to DATA_3 [A] |         | R4                    |        |        |        |

Table 190

(see 3.5.1.14 Set current / trip (single write- and single/ multiple single read-write access) Single access also)

### 3.5.3.10 SetOnOffAllChannels (group write- / read-write access)

EDCP frame:

| Access                | DATA_DIR                                                                           | DATA_ID | DATA_3         | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|------------------------------------------------------------------------------------|---------|----------------|--------|--------|--------|
| master group write    | 0                                                                                  | 0x2200  | SetOnOffAllChs |        |        |        |
| master group read-    | 1                                                                                  | 0x2200  |                |        |        |        |
| HV board write access | 0                                                                                  | 0x2200  | SetOnOffAllChs |        |        |        |
| Notes:                |                                                                                    |         |                |        |        |        |
| SetOnOffAllChs        | DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) |         |                |        |        | UI4    |
| SetOnOffAllChs        | DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment)             |         |                |        |        | UI2    |

Table 191

| Bit31 | Bit30 | Bit29 | Bit28 | Bit27 | Bit26 | Bit25 | Bit24 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CH31  | CH30  | CH29  | CH28  | CH27  | CH26  | CH25  | CH24  |
| Bit23 | Bit22 | Bit21 | Bit20 | Bit19 | Bit18 | Bit17 | Bit16 |
| CH23  | CH22  | CH21  | CH20  | CH19  | CH18  | CH17  | CH16  |
| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit09 | Bit08 |
| CH15  | CH14  | CH13  | CH12  | CH11  | CH10  | CH9   | CH8   |
| Bit07 | Bit06 | Bit05 | Bit04 | Bit03 | Bit02 | Bit01 | Bit00 |
| CH7   | CH6   | CH5   | CH4   | CH3   | CH2   | CH1   | CH0   |

Table 192

SetOnOffAllChs    DATA\_0 to DATA\_1 for channel 0 to channel 15    UI2

CHm = 1            Channel ON

CHm = 0            Channel OFF

The SetOnOffAllChs represents a 32 bit field to control the channel property setON for each channel member of the bit field with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to setON for all channel members simultaneously with on instruction.

### 3.5.3.11 SetEmergencyAllChannels (group write- / read-write access)

EDCP frame:

| Access                | DATA_DIR                                                                           | DATA_ID | DATA_3             | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|------------------------------------------------------------------------------------|---------|--------------------|--------|--------|--------|
| master group write    | 0                                                                                  | 0x2201  | SetEmergencyAllChs |        |        |        |
| master group read-    | 1                                                                                  | 0x2201  |                    |        |        |        |
| HV board write access | 0                                                                                  | 0x2201  | SetEmergencyAllChs |        |        |        |
| Notes:                |                                                                                    |         |                    |        |        |        |
| SetEmergencyAllChs    | DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) |         |                    |        |        | UI4    |
| SetEmergencyAllChs    | DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment)             |         |                    |        |        | UI2    |

Table 193

| Bit31 | Bit30 | Bit29 | Bit28 | Bit27 | Bit26 | Bit25 | Bit24 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CH31  | CH30  | CH29  | CH28  | CH27  | CH26  | CH25  | CH24  |
| Bit23 | Bit22 | Bit21 | Bit20 | Bit19 | Bit18 | Bit17 | Bit16 |
| CH23  | CH22  | CH21  | CH20  | CH19  | CH18  | CH17  | CH16  |
| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit09 | Bit08 |
| CH15  | CH14  | CH13  | CH12  | CH11  | CH10  | CH9   | CH8   |
| Bit07 | Bit06 | Bit05 | Bit04 | Bit03 | Bit02 | Bit01 | Bit00 |
| CH7   | CH6   | CH5   | CH4   | CH3   | CH2   | CH1   | CH0   |

Table 194

SetEmergencyAllChs      DATA\_0 to DATA\_1 for channel 0 to channel 15    UI2

CHm = 1 Channel EMERGENCY set

CHm = 0 Channel EMERGENCY reset

The 'SetEmergencyAllChs' represents a 32 bit field to control the channel property 'setEMCY' for each channel member of the bit field with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to 'setEMCY' for all channel members simultaneously with on instruction.

### 3.5.3.12 EventStatusVLimitAllChannels (group write- / read-write access)

EDCP frame:

| Access                  | DATA_DIR                                                                           | DATA_ID | DATA_3                  | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|------------------------------------------------------------------------------------|---------|-------------------------|--------|--------|--------|
| master group write      | 0                                                                                  | 0x2202  | EventStatusVLimitAllChs |        |        |        |
| master group read-      | 1                                                                                  | 0x2202  |                         |        |        |        |
| HV board write access   | 0                                                                                  | 0x2202  | EventStatusVLimitAllChs |        |        |        |
| Notes:                  |                                                                                    |         |                         |        |        |        |
| EventStatusVLimitAllChs | DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) |         |                         |        |        | UI4    |
| EventStatusVLimitAllChs | DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment)             |         |                         |        |        | UI2    |

Table 195

| Bit31 | Bit30 | Bit29 | Bit28 | Bit27 | Bit26 | Bit25 | Bit24 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CH31  | CH30  | CH29  | CH28  | CH27  | CH26  | CH25  | CH24  |
| Bit23 | Bit22 | Bit21 | Bit20 | Bit19 | Bit18 | Bit17 | Bit16 |
| CH23  | CH22  | CH21  | CH20  | CH19  | CH18  | CH17  | CH16  |
| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit09 | Bit08 |
| CH15  | CH14  | CH13  | CH12  | CH11  | CH10  | CH9   | CH8   |
| Bit07 | Bit06 | Bit05 | Bit04 | Bit03 | Bit02 | Bit01 | Bit00 |
| CH7   | CH6   | CH5   | CH4   | CH3   | CH2   | CH1   | CH0   |

Table 196

EventStatusVLimitAllChs      DATA\_0 to DATA\_1 for channel 0 to channel 15      UI2

CHm = 1      Channel event status voltage limit

CHm = 0      nothing

The 'EventStatusVLimitAllChs' represents a 32 bit field to control the channel property 'EVLIM' for each channel with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to reset 'EVLIM' for all channel members simultaneously with one instruction.

If the voltage limit was exceeded or an external over voltage occurs at the channel output (i.e. Output voltage → Set voltage) then the channel will be switched off and the according bit will be set. The error bits will be canceled and the voltage of the corresponding channel can be switched on again only after writing 'EventStatusVLimitAllChs' with the bits, which are corresponding to the channel errors are set to "1".

### 3.5.3.13 EventStatusCurrentLimitAllChannels (group write- / read-write access)

EDCP frame:

| Access                  | DATA_DIR                                                                           | DATA_ID | DATA_3                  | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|------------------------------------------------------------------------------------|---------|-------------------------|--------|--------|--------|
| master group write      | 0                                                                                  | 0x2203  | EventStatusCLimitAllChs |        |        |        |
| master group read-      | 1                                                                                  | 0x2203  |                         |        |        |        |
| HV board write access   | 0                                                                                  | 0x2203  | EventStatusCLimitAllChs |        |        |        |
| Notes:                  |                                                                                    |         |                         |        |        |        |
| EventStatusCLimitAllChs | DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) |         |                         |        |        | UI4    |
| EventStatusCLimitAllChs | DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment)             |         |                         |        |        | UI2    |

Table 197

| Bit31 | Bit30 | Bit29 | Bit28 | Bit27 | Bit26 | Bit25 | Bit24 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CH31  | CH30  | CH29  | CH28  | CH27  | CH26  | CH25  | CH24  |
| Bit23 | Bit22 | Bit21 | Bit20 | Bit19 | Bit18 | Bit17 | Bit16 |
| CH23  | CH22  | CH21  | CH20  | CH19  | CH18  | CH17  | CH16  |
| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit09 | Bit08 |
| CH15  | CH14  | CH13  | CH12  | CH11  | CH10  | CH9   | CH8   |
| Bit07 | Bit06 | Bit05 | Bit04 | Bit03 | Bit02 | Bit01 | Bit00 |
| CH7   | CH6   | CH5   | CH4   | CH3   | CH2   | CH1   | CH0   |

Table 198

EventStatusCLimitAllChs DATA\_0 to DATA\_1 for channel 0 to channel 15 UI2

CHm = 1 Channel event status current limit

CHm = 0 nothing

The EventStatusCLimitAllChs represents a 32 bit field to control the channel property ECLIM for each channel with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to reset ECLIM for all channel members simultaneously with on instruction.

The module responds to the exceeding of the hardware current limit which has been set in the channel in dependence on the according setKILena bit of module control as follows:

- setKILena = 1: Voltage will be switched off permanently without ramp, green LED on front panel is off until a write of 'EventStatusCLimitAllChs' with the bits, which are corresponding to the channel errors set to "1". The error bits will be cancelled and the voltage of the corresponding channels can be switched on again.
- setKILena = 0: HV modules without a current control E16D0, E16D1 and E08B0 will be switched off voltage without ramp, green LED on front panel is off. If the output voltage arrives at 0 V the ramping to set voltage will be started automatically again. The green LED again flash only after writing the 'EventStatusCLimitAllChs' with the respective bits.

HV modules with a current control will not switch off high voltage and operate in constant current mode, green LED on front panel is off. The output current will be limited. The green LED flashes only after writing of EventStatusCLimitAllChs with the respective bits and removing of the limitation of current before.

### 3.5.3.14 EventStatusCurrentTripAllChannels (group write- / read-write access)

EDCP frame:

| Access                | DATA_DIR                                                                           | DATA_ID | DATA_3               | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|------------------------------------------------------------------------------------|---------|----------------------|--------|--------|--------|
| master group write    | 0                                                                                  | 0x2204  | EventStatusTrpAllChs |        |        |        |
| master group read-    | 1                                                                                  | 0x2204  |                      |        |        |        |
| HV board write access | 0                                                                                  | 0x2204  | EventStatusTrpAllChs |        |        |        |
| Notes:                |                                                                                    |         |                      |        |        |        |
| EventStatusTrpAllChs  | DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) |         |                      |        |        | UI4    |
| EventStatusTrpAllChs  | DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment)             |         |                      |        |        | UI2    |

Table 199

| Bit31 | Bit30 | Bit29 | Bit28 | Bit27 | Bit26 | Bit25 | Bit24 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CH31  | CH30  | CH29  | CH28  | CH27  | CH26  | CH25  | CH24  |
| Bit23 | Bit22 | Bit21 | Bit20 | Bit19 | Bit18 | Bit17 | Bit16 |
| CH23  | CH22  | CH21  | CH20  | CH19  | CH18  | CH17  | CH16  |
| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit09 | Bit08 |
| CH15  | CH14  | CH13  | CH12  | CH11  | CH10  | CH9   | CH8   |
| Bit07 | Bit06 | Bit05 | Bit04 | Bit03 | Bit02 | Bit01 | Bit00 |
| CH7   | CH6   | CH5   | CH4   | CH3   | CH2   | CH1   | CH0   |

Table 200

EventStatusTrpAllChs      DATA\_0 to DATA\_1 for channel 0 to channel 15    UI2

CHm = 1                      Channel event status trip

CHm = 0                      nothing

The 'EventStatusTrpAllChs' represents a 32 bit field to control the channel property ETRP for each channel with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to reset ETRP for all channel members simultaneously with on instruction.

If the output current exceeds the programmed current trip value then the corresponding bits will be set:

setKILena = 1:      Voltage will be switched off permanently without ramp, green LED on front panel is off until a write of 'EventStatusTrpAllChs' with the bits, which are corresponding to the channel errors set to "1". The error bits will be cancelled and the voltage of the corresponding channels can be switched on again.

setKILena = 0:      HV will not be switched but the green LED on front panel is off. The output current will be limited if there is a current control. The green LED flashes only after writing of 'EventStatusTrpAllChs' with the respective bits and removing of the limitation of current before.

### 3.5.3.15 EventStatusExternalInhibitAllChannels (group write- / read-write access)

EDCP frame:

| Access                | DATA_DIR                                                                           | DATA_ID | DATA_3               | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|------------------------------------------------------------------------------------|---------|----------------------|--------|--------|--------|
| master group write    | 0                                                                                  | 0x2205  | EventStatusInhAllChs |        |        |        |
| master group read-    | 1                                                                                  | 0x2205  |                      |        |        |        |
| HV board write access | 0                                                                                  | 0x2205  | EventStatusInhAllChs |        |        |        |
| Notes:                |                                                                                    |         |                      |        |        |        |
| EventStatusInhAllChs  | DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) |         |                      |        |        | UI4    |
| EventStatusInhAllChs  | DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment)             |         |                      |        |        | UI2    |

Table 201

| Bit31 | Bit30 | Bit29 | Bit28 | Bit27 | Bit26 | Bit25 | Bit24 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CH31  | CH30  | CH29  | CH28  | CH27  | CH26  | CH25  | CH24  |
| Bit23 | Bit22 | Bit21 | Bit20 | Bit19 | Bit18 | Bit17 | Bit16 |
| CH23  | CH22  | CH21  | CH20  | CH19  | CH18  | CH17  | CH16  |
| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit09 | Bit08 |
| CH15  | CH14  | CH13  | CH12  | CH11  | CH10  | CH9   | CH8   |
| Bit07 | Bit06 | Bit05 | Bit04 | Bit03 | Bit02 | Bit01 | Bit00 |
| CH7   | CH6   | CH5   | CH4   | CH3   | CH2   | CH1   | CH0   |

Table 202

EventStatusInhAllChs      DATA\_0 to DATA\_1 for channel 0 to channel 15    UI2

CHm = 1                      Channel event status inhibit

CHm = 0                      nothing

The 'EventStatusInhAllChs' represents a 32 bit field to control the channel property ETRP for each channel with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to reset ETRP for all channel members simultaneously with one instruction.

Voltage will be switched off permanently without ramp, if the INHIBIT is active, the green LED on front panel is off. When the INHIBIT is going back from active to passive state then the INHIBIT flag have to be erased by write of the 'EventStatusInhAllChs' before the voltage can be switched on again. The INHIBIT flags are reset with set of the corresponding channel bit to "1".

### 3.5.3.16 Set ON / OFF channels extender (group write- / read-write access)

EDCP frame:

| Access                | DATA_DIR                                                                           | DATA_ID | DATA_3              | DATA_2 | DATA_1 | DATA_0 |
|-----------------------|------------------------------------------------------------------------------------|---------|---------------------|--------|--------|--------|
| master group write    | 0                                                                                  | 0x2280  | SetOnOffChsExtender |        |        |        |
| master group read-    | 1                                                                                  | 0x2280  |                     |        |        |        |
| HV board write access | 0                                                                                  | 0x2280  | SetOnOffChsExtender |        |        |        |
| Notes:                |                                                                                    |         |                     |        |        |        |
| SetOnOffAllChs        | DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) |         |                     |        |        | UI4    |
| SetOnOffAllChs        | DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment)             |         |                     |        |        | UI2    |

Table 203

| Bit31 | Bit30 | Bit29 | Bit28 | Bit27 | Bit26 | Bit25 | Bit24 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CH63  | CH62  | CH61  | CH60  | CH59  | CH58  | CH57  | CH56  |
| Bit23 | Bit22 | Bit21 | Bit20 | Bit19 | Bit18 | Bit17 | Bit16 |
| CH55  | CH54  | CH53  | CH52  | CH51  | CH50  | CH49  | CH48  |
| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit09 | Bit08 |
| CH47  | CH46  | CH45  | CH44  | CH43  | CH42  | CH41  | CH40  |
| Bit07 | Bit06 | Bit05 | Bit04 | Bit03 | Bit02 | Bit01 | Bit00 |
| CH39  | CH38  | CH37  | CH36  | CH36  | CH34  | CH33  | CH32  |

Table 204

SetOnOffAllChs DATA\_0 to DATA\_1 for channel 0 to channel 15 UI2

CHm = 1 Channel ON

CHm = 0 Channel OFF

The 'SetOnOffChsExtender' represents a 32 bit field to control the channel property 'setON' for each channel member of the bit field with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to 'setON' for all channel members simultaneously with on instruction.

### 3.5.3.17 Set EMERGENCY channels extender (group write- / read-write access)

EDCP frame:

| Access                  | DATA_DIR                                                                           | DATA_ID | DATA_3                  | DATA_2 | DATA_1 | DATA_0 |
|-------------------------|------------------------------------------------------------------------------------|---------|-------------------------|--------|--------|--------|
| master group write      | 0                                                                                  | 0x2201  | SetEmergencyChsExtender |        |        |        |
| master group read-      | 1                                                                                  | 0x2201  |                         |        |        |        |
| HV board write access   | 0                                                                                  | 0x2201  | SetEmergencyChsExtender |        |        |        |
| Notes:                  |                                                                                    |         |                         |        |        |        |
| SetEmergencyChsExtender | DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) |         |                         |        |        | UI4    |
| SetEmergencyChsExtender | DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment)             |         |                         |        |        | UI2    |

Table 205

| Bit31 | Bit30 | Bit29 | Bit28 | Bit27 | Bit26 | Bit25 | Bit24 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CH63  | CH62  | CH61  | CH60  | CH59  | CH58  | CH57  | CH56  |
| Bit23 | Bit22 | Bit21 | Bit20 | Bit19 | Bit18 | Bit17 | Bit16 |
| CH55  | CH54  | CH53  | CH52  | CH51  | CH50  | CH49  | CH48  |
| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit09 | Bit08 |
| CH47  | CH46  | CH45  | CH44  | CH43  | CH42  | CH41  | CH40  |
| Bit07 | Bit06 | Bit05 | Bit04 | Bit03 | Bit02 | Bit01 | Bit00 |
| CH39  | CH38  | CH37  | CH36  | CH36  | CH34  | CH33  | CH32  |

Table 206

SetEmergencyChsExtender DATA\_0 to DATA\_1 for channel 0 to channel 15 UI2

CHm = 1 Channel EMERGENCY set

CHm = 0 Channel EMERGENCY reset

The 'SetEmergencyChsExtender' represents a 32 bit field to control the channel property 'setEMCY' for each channel member of the bit field with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to 'setON' for all channel members simultaneously with on instruction.

## 3.5.4 Important DCP Module Accesses

### 3.5.4.1 GeneralStatus (group write- / read-write / active access)

DCP frame:

| Access                 | EXT_INSTR | DATA_DIR | DATA_ID | DATA_1        | DATA_0  |
|------------------------|-----------|----------|---------|---------------|---------|
| HV board active access | 0         | 0        | 0xc0    | GeneralStatus | Details |
| Notes:                 |           |          |         |               |         |
| GeneralStatus          | DATA_1    |          |         | UI1           |         |

Table 207

| b15  | b14                    | b13       | b12  | b11  | b10   | b9     | b8       |
|------|------------------------|-----------|------|------|-------|--------|----------|
| Save | KILLena/<br>HwVLnotLow | SPLYTMPgd | AvAd | Stbl | SFLPg | noRamp | noSumErr |
| b7   | b6                     | b5        | b4   | b3   | b2    | b1     | b0       |
| INHb | BordTemp               | res       | res  | VLIM | CLIM  | RERR   | TRP      |

Table 208

Details DATA\_0 UI1

#### GeneralStatus:

| Bit        | Name                       | Description                                                                              |
|------------|----------------------------|------------------------------------------------------------------------------------------|
| Save       | Save                       | save function bit stored permanently the current set values (takes some seconds ca. 10s) |
| KILLena    | KillEnable                 | kill function bit                                                                        |
| HwVLnotLow | HardwareVoltageLimitNotLow | hardware voltage limit is not to low bit, for device class 21 only                       |
| SPLYTMPgd  | SupplyGoodTemperatureGood  | supply good and board temperature good bit                                               |
| AvAd       | AverageAdjust              | average and fine adjustment bit                                                          |
| SFLPg      | SafetyLoop                 | safety loop bit                                                                          |
| noRamp     | noRamp                     | flag to display that no voltage is ramping                                               |
| noSumErr   | NoSumError                 | displays that there has been built a sum error flag by VLIM&ILIM&TRP over all channels   |

Table 209

**Details:**

| Bit       | Name                 | Description                                                        |
|-----------|----------------------|--------------------------------------------------------------------|
| INHB      | Inhibit              | an external INHIBIT at least one of the channels (device class 25) |
| BoardTemp | BoardTemperatureGood | board temperature is good                                          |
| VLIM      | VoltageLimit         | hardware voltage limit has been exceeded                           |
| CLIM      | CurrentLimit         | hardware current limit has been exceeded                           |
| RERR      | RegulationError      | regulation error, for device class 21 only                         |
| TRP       | Trip                 | voltage or current trip                                            |
| res       | reserved             |                                                                    |

| Bit            | Description                                                                                                                                  |
|----------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| Save=0         | no write access to EEPROM                                                                                                                    |
| Save=1         | store all set values to EEPROM (time to save ca. 10s) for device classes 24 and 25 only                                                      |
| KILLena=0      | kill function disable                                                                                                                        |
| KILLena = 1    | kill function enable, for device classes 21 only                                                                                             |
| HwVLnotLow = 0 | HW Vlimit voltage limit is too low, it is not possible to switch on the HV, reset by write with HwVLtoLow flag is set to "1"                 |
| HwVLnotLow = 1 | HW Vlimit in proper range                                                                                                                    |
| SPLYTMPgd = 0  | supply voltages are out of range or module temperature > 55°C                                                                                |
| SPLYTMPgd = 1  | supply voltages are in range and module temperature ≤ 55°C                                                                                   |
| AvAd = 0       | fine adjustment and average of voltage, current measurement OFF                                                                              |
| AvAd = 1       | fine adjustment and average of voltage, current measurement ON                                                                               |
| Stbl = 0       | all channels are stable with program ADC filter frequency fN. (ADC conversion time = 1/fN, see 'Set ADC filter frequency', default fN=50 Hz) |
| Stbl = 1       | at least one channel is ramping Vo or not yet stable after ramping (ramping - with ADC filter frequency fN=100 Hz)                           |
| SFLPgd = 0     | safety loop is broken -VO has been shut off, reset by a write of the 'General status' with sloop flag is set to "1"                          |
| SFLPgd = 1     | safety loop is closed                                                                                                                        |
| noRamp = 0     | VO is ramping in at least one channel                                                                                                        |
| noRamp = 1     | no channel is ramping                                                                                                                        |
| noSumErr = 0   | voltage limit, current limit or trip has been exceeded in at least one of the channels (error)                                               |
| noSumErr = 1   | status channel flags v & c & t = 0 for all channels (no errors)                                                                              |
| INHB = 0       | no external INHIBIT signal                                                                                                                   |
| INHB = 1       | external INHIBIT signal                                                                                                                      |
| BoardTemp = 0  | temperature ≤ 55°C                                                                                                                           |
| BoardTemp = 1  | temperature > 55°C                                                                                                                           |
| VLIM=0         | hardware voltage limit hasn't been exceeded                                                                                                  |
| VLIM=1         | hardware voltage limit has been exceeded                                                                                                     |
| CLIM=0         | hardware current limit hasn't been exceeded                                                                                                  |
| CLIM=1         | hardware current limit has been exceeded                                                                                                     |
| RERR=0         | hardware current hasn't been exceeded                                                                                                        |
| RERR=1         | voltage has been exceeded                                                                                                                    |

|       |                         |
|-------|-------------------------|
| TRP=0 | no trip                 |
| TRP=1 | voltage or current trip |

Table 210

If one of the bits 'noHwVLtoLow', 'SPLYTMPgd', 'SFLPg d', 'noSumErr' in the modul access "General status module" has not been set, the module will send this access as an active error message with higher priority (ID9=0). An additional 2nd data byte offers more information about the NoSumError flag of the first byte.

Example of an active error message

| access                 | identifier | length code | DATA_ID | DATA_1 | DATA_0 |
|------------------------|------------|-------------|---------|--------|--------|
| HV board active access | 0x180      | 3           | 0xc0    | 0x57   | 0x01   |

Table 211

↓ TRP=1 ↓ noSumErr=0 etc. (3.5.4.1 General Status)

### 3.5.4.2 Log-on / Log-off Front-end device at superior layer (module active- / write access)

DCP frame:

| Access                 | DATA_DIR | DATA_ID | DATA_1                                                                          | DATA_0      |
|------------------------|----------|---------|---------------------------------------------------------------------------------|-------------|
| HV board active access | 1        | 0xD8    | GeneralStatus                                                                   | DeviceClass |
| master write access    | 0        | 0xD8    | LogOnOff                                                                        |             |
| Notes:                 |          |         |                                                                                 |             |
| GeneralStatus          | DATA_1   | UI1     | refer chapter 3.5.4.1 GeneralStatus (group write- / read-write / active access) |             |
| DeviceClass            | DATA_0   | UI1     |                                                                                 |             |

Table 212

| device class         |                  | label       | firmware                            | description                                                                       | associated serial numbers              |
|----------------------|------------------|-------------|-------------------------------------|-----------------------------------------------------------------------------------|----------------------------------------|
| EDCP                 | DCP              |             |                                     |                                                                                   |                                        |
| 21                   | 0                | EDS         | E16D0_xxx<br>E16D1_xxx<br>E24D1_xxx | EDS 16 channels per PCB<br>EDS 16 channels per PCB<br>EDS 24 channels per PCB     | 471xxx / 71xxxx                        |
| 22                   | -                | HPS / LPS   | H101C0_5xx                          | HPS 19", 1 channel HV Power Supply (300W, 800W)                                   | 68xxxx / 70xxxx                        |
| 23                   | -                | HPS / LPS   | H201C0_2xx                          | HPS compact,1 channel HV Power Supply (350W)                                      | 68xxxx / 70xxxx                        |
| 24<br>24<br>25<br>25 | 6<br>6<br>7<br>7 | EHS/EMS/ELS | E08C0_xxx                           | ExS 8 channel per PCB, standard common GND                                        | 73xxxx<br>73xxxxx<br>74xxxx<br>74xxxxx |
| 25                   | 7                | EHS/EMS/ELS | E08F0_xxx                           | ExS 8 channel per PCB, standard, floating GND                                     | 474xxx                                 |
| 26                   | 2                | EHS/EMS/ELS | E08F2_xxx                           | ExS 8 channel per PCB, floating GND<br>2 ranges for measurement of current        | 72xxxx<br>72xxxxx                      |
| 27                   | -                | EHS/EMS/ELS | E08C2_xxx                           | ExS 8 channel per PCB, common floating GND<br>2 ranges for measurement of current | 78xxxx<br>78xxxxx                      |
| 41                   | -                | MICC        | MICC_3xx                            | MICC Multichannel Interface Crate Controller for MMC Crates                       | 458xxx                                 |
| 42                   | -                | MICP        | MICP_3xx                            | MICP Multichannel Interface Crate PHQ Controller for MMC Crates                   | 458xxx                                 |
| 60                   | -                | HPS         | H101C1_1xx                          | HPS 19", 1 channel HV Power Supply (1.5kW – 10 kW)                                | 90xxxxx                                |
| 70                   | -                | EHS         | E16C1_1xx                           | ExS 16 channels per PCB or 32 channels per module                                 | 79xxxx<br>79xxxxx                      |

Table 213

LogOnOff                      DATA\_1=1 superior layer send a "Log-on" at Front-end device to registration    UI1  
                                    DATA\_1=0 superior layer send "Log-off" to Front-end device  
                                    xxx and xxxx are running numbers

After POWER ON the Front-end device - up to a number of two per module - will give this module access cyclically on the bus (ca. 1 sec). If a controller of superior layer identifies this access then it is possible to register this as a Front-end device and is possible to address it with FE\_ADR. (see also description 11 bit-Identifier)

After the successful registration the Front-end device will not send further 'Log-on' accesses as long as:

- it receives accesses from the external CAN Bus in periods shorter than one minute or
- until the superior controller will send a 'Log-off' access to the Front-end device.

### 3.5.5 Events

The module provides an extended event collecting logic. This is necessary to monitor extraordinary events and forward them to the host.

#### 3.5.5.1 Channel events

These event-bits in the channel event status register are related to mask bits in the channel event mask register. With help of an AND function (bit-wise) between an event bit and the according mask bit a result only occurs where the mask bit has been set. A following logic OR function of all of these results leads to the event status of the channels.

```
ModuleEventChannelStatus[ch] = (ChannelEventStatus.EVLIM[ch] AND ChannelEventMask.MEVLIM[ch]) OR
see 3.5.2.9                  (ChannelEventStatus.ECLIM[ch] AND ChannelEventMask.MECLIM[ch]) OR
ModuleEventChannelStatus    (ChannelEventStatus.ETRP[ch] AND ChannelEventMask.METRP[ch]) OR
(module write- / read-write  (ChannelEventStatus.EEINH[ch] AND ChannelEventMask.MEEINH[ch]) OR
access)                     (ChannelEventStatus.EVBNDs[ch] AND ChannelEventMask.MEVBNDS[ch]) OR
                             (ChannelEventStatus.ECBNDs[ch] AND ChannelEventMask.MECBNDs[ch]) OR
                             (ChannelEventStatus.ECV[ch] AND ChannelEventMask.MECV[ch]) OR
                             (ChannelEventStatus.ECC[ch] AND ChannelEventMask.MECC[ch]) OR
                             (ChannelEventStatus.EEMCY[ch] AND ChannelEventMask.MEEMCY[ch]) OR
                             (ChannelEventStatus.EEOR[ch] AND ChannelEventMask.MEEOR[ch]) OR
                             (ChannelEventStatus.EOn2Off[ch] AND ChannelEventMask.MEOn2Off [ch]) OR
                             (ChannelEventStatus.EIER[ch] AND ChannelEventMask.MEIER[ch])
ch={0..n}
```

The status of all channel events is collected in the register EventChannelStatus of the module items.

For a selection or filtering of the channel events a related mask register has been provided (3.5.2.11 ModuleEventChannelMask (module write- / read-write access)). With help of the AND or OR function (see channel) the event active signal of the channels EventChannelActive will be generated:

```
EventChannelActive          = (EventChannelStatus[0] AND EventChannelMask[0]) OR
                             (EventChannelStatus[1] AND EventChannelMask[1]) OR
                             ...
                             (EventChannelStatus[n] AND EventChannelMask[n])
```

### 3.5.5.2 Group events (in preparation)

Like written before groups are also able to generate Events. These events will be collected in the status word EventGroupStatus of the GroupData. With help of the mask register EventGroupMask the event active signal of the groups EventGroupActive will be generated.

$$\begin{aligned} \text{EventGroupActive} &= (\text{EventGroupStatus}[0] \text{ AND } \text{EventGroupMask}[0]) \text{ OR} \\ &(\text{EventGroupStatus}[1] \text{ AND } \text{EventGroupMask}[1]) \text{ OR} \\ &\dots \\ &(\text{EventGroupStatus}[23] \text{ AND } \text{EventGroupMask}[24]) \end{aligned}$$

### 3.5.5.3 Module events

With help of the NOT, AND or OR function the event active signal of the module EventModuleActive will be generated:

$$\begin{aligned} \text{EventModuleActive} &= (\text{NOT}(\text{ModuleEventStatus.ETMPngd}) \text{ AND } \text{ChannelEventMask.METMPngd}) \text{ OR} \\ &(\text{NOT}(\text{ModuleEventStatus.ESPLYngd}) \text{ AND } \text{ChannelEventMask.MESPLYngd}) \text{ OR} \\ &(\text{NOT}(\text{ModuleEventStatus.ESFLPngd}) \text{ AND } \text{ModuleEventMask.MESFLPngd}) \text{ OR} \end{aligned}$$

From both signals EventChannelActive and EventModuleActive the global event active signal of the module IsEventActive of the ModuleStatus register will be generated.

$$\text{IsEventActive} = (\text{EventChannelActive} \text{ OR } \text{EventGroupActive} \text{ OR } \text{EventModuleActive})$$

This global signal 'IsEventActive' triggers a fast message on the CAN bus with the DCP Module frame of General status.

Example to generate fast error messages:

The event flag ECC of the ChannelEventStatus for channel 2 or the event flag EventTemperatureNotGood of the ModuleEventStatus should release a fast CAN frame:

- Channel[2].ChannelEventMask.Bit.MECC = 1
- Module.EventChannelMask.Bit.2 = 1
- Module.EventMask.Bit.METMPngd = 1

The signal isEvtActive is triggered and releases a fast CAN frame of General status when:

(Channel[2].ChannelEventStatus.Bit.ECC & Channel[2].ChannelEventMask.Bit.MECC & Module.ModuleEventChannelMask.Bit2

OR

Module.ModuleEventStatus.Bit.ETMPngd & Module.ModuleEventMask.Bit.METMPngd

OR

(Module.ModuleEventChannelStatus.Bit2 & Module.ModuleEventChannelMask.Bit2 )

Fast CAN frame in case of Channel[2].ChannelEventStatus.Bit.ECC == 1:

0x190 3 0xc0 0x37 0x00 (ID=0x190, ID9=0; Len=3; DATA\_ID=0xc0; Data=0x3700)

(Channel[2].ChannelEventStatus.Bit.ECC & Channel[2].ChannelEventMask.Bit.MECC)==1 → ModuleEventChannelStatus.Bit2=1

Fast CAN frame in case of Module.ModuleEventStatus.Bit. ETMPngd == 1:

0x190 3 0xc0 0x17 0x40 (ID=0x190, ID9=0; Len=3; DATA\_ID=0xc0; Data= 0x1740)

#### INFORMATION



INFORMATION

Please note that, a release of a fast CAN frame is different in handling depending on EDCP or DCP mode!

## 4 Appendix

### 4.1 A – Shortcuts

|         |                                                                                                                              |
|---------|------------------------------------------------------------------------------------------------------------------------------|
| BCD     | binary coded decimal format                                                                                                  |
| CAN     | controller area network                                                                                                      |
| Chm     | channel m = 0 ... 47                                                                                                         |
| CHN     | channel                                                                                                                      |
| DCP     | device control protocol                                                                                                      |
| DATA_ID | data identifier of DCP                                                                                                       |
| fN      | first filter notch frequency                                                                                                 |
| HV      | High voltage                                                                                                                 |
| HW      | hardware                                                                                                                     |
| IEEE488 | Is a short-range digital communications 8-bit parallel multi-master interface bus specification developed by Hewlett Packard |
| Imeas   | Current Measure, the actual measured output current                                                                          |
| Imax    | Hardware current limit                                                                                                       |
| IO max  | Nominal current                                                                                                              |
| Iset    | Set current                                                                                                                  |
| Itrip   | Trip current                                                                                                                 |
| ISO     | International Standard Organization                                                                                          |
| LSB     | least significant bit                                                                                                        |
| MBR     | channel members                                                                                                              |
| MSB     | most significant bit                                                                                                         |
| NBR     | group number                                                                                                                 |
| NMT     | network management service                                                                                                   |
| OSI     | Open System Interconnect                                                                                                     |
| PCB     | printed circuit board                                                                                                        |
| p/a     | passive / active                                                                                                             |
| SN.     | serial number                                                                                                                |
| USB     | Universal Serial Bus                                                                                                         |
| UI1     | unsigned character                                                                                                           |
| SI1     | signed character                                                                                                             |
| UI2     | unsigned short integer (16 bit)                                                                                              |
| UI4     | unsigned integer (32 bit)                                                                                                    |
| R4      | float according to IEEE-754 single precision format                                                                          |
| Vmeas   | Voltage Measure, the actual measurement output voltage                                                                       |
| Vmax    | Hardware voltage limit                                                                                                       |
| VO max  | Nominal voltage                                                                                                              |
| Vset    | Set voltage                                                                                                                  |
| SW      | software                                                                                                                     |

## 4.2 Appendix B – Diagram of operating modes

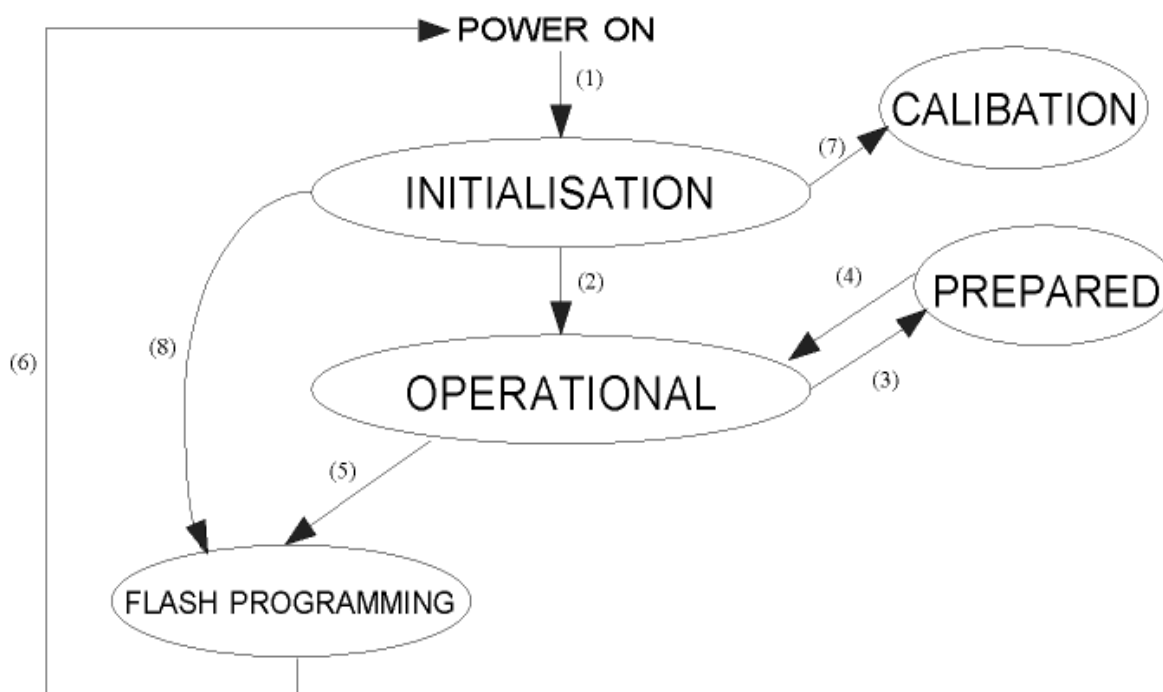


Figure 1

- (1) The INITIALISATION follows after the POWER ON reset of the device hardware. It can be differ between different device classes.
- (2) The state OPERATIONAL will be obtained by the device itself if all initializations are ready or the state PREPARED runs in time out.
- (3) NMT Stop switches the devices of the CAN segment into the state PREPARED. In this state the permanent settings of the devices can be changed (per device Bit rate, Set voltage, Set current, Ramp speed, General status, Threshold to arm the errors detection, Discharge relay configuration, CAN message configuration and additional the Bit rate as a broadcast message).
- (4) NMT Start takes the devices of the CAN segment back to the OPERATIONAL state.
- (5) With the special Flash programming access the device runs into the state FLASH PROGRAMMING. The high voltage will be switched off automatically before.
- (6) The device will execute a POWER ON reset itself at the end of FLASH PROGRAMMING.
- (7) The state CALIBRATION will be obtained by setting of the corresponding switches at the Calibration Crate.
- (8) The state FLASH Programming will be obtained also if the corresponding switch at the Calibration Crate / Flash Programming Slot are set.

### 4.3 Appendix C – Programming flowchart to store the settings permanently with help of General state save bit

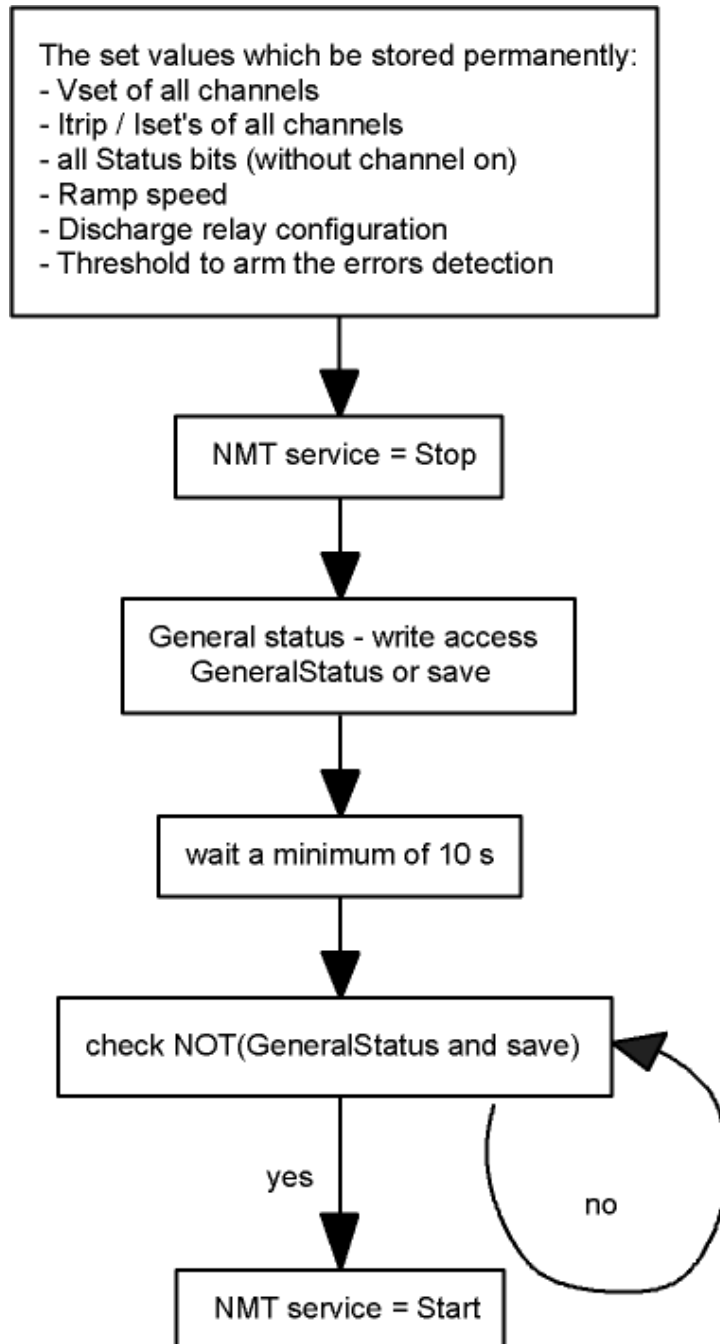


Figure 2

#### 4.4 Appendix D – Programming flowchart to store the configurations of the module permanently with help of General state save bit

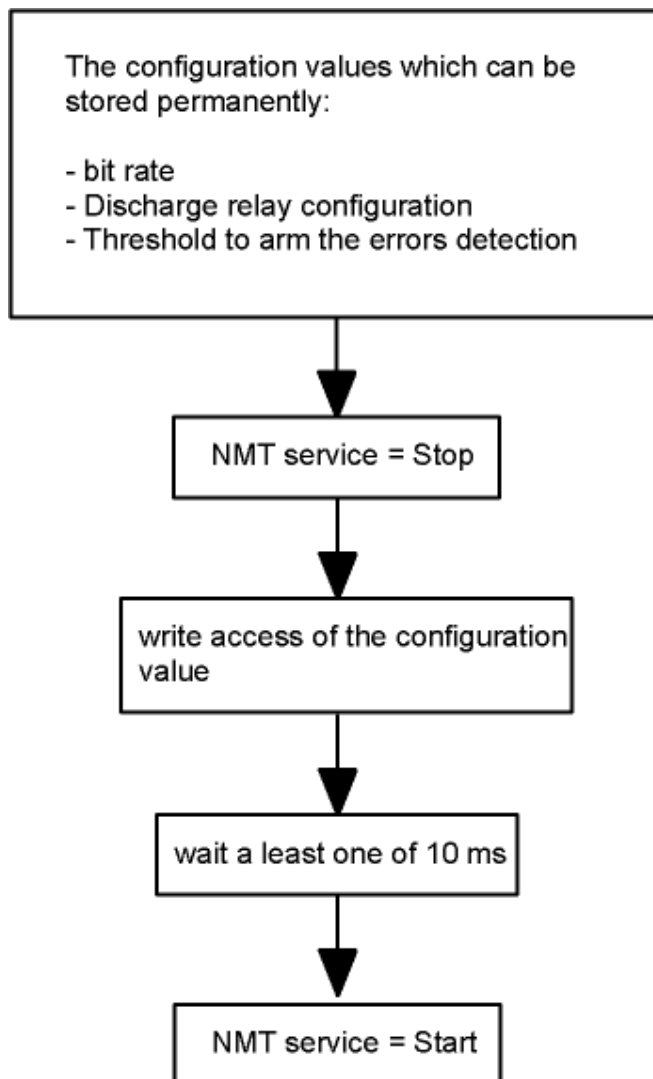


Figure 3

## 4.5 Appendix E – Literature references

|                                                                                                                                                                                     |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>This document</b>                                                                                                                                                                |
| <a href="https://iseg-hv.com/download/?dir=SOFTWARE/SNMPguide/SNMP_Programmers-Guide_en.pdf">https://iseg-hv.com/download/?dir=SOFTWARE/SNMPguide/SNMP_Programmers-Guide_en.pdf</a> |
| <b>iseg Hardware Abstraction Layer</b>                                                                                                                                              |
| <a href="http://download.iseg-hv.com/SYSTEMS/MMS/isegHardwareAbstractionLayer.pdf">http://download.iseg-hv.com/SYSTEMS/MMS/isegHardwareAbstractionLayer.pdf</a>                     |
| <b>CAN data link layers in some detail</b>                                                                                                                                          |
| <a href="https://www.can-cia.org/can-knowledge/can/can-data-link-layers/">https://www.can-cia.org/can-knowledge/can/can-data-link-layers/</a>                                       |
| <b>High Voltage System module</b>                                                                                                                                                   |
| <a href="https://iseg-hv.com/">https://iseg-hv.com/</a>                                                                                                                             |
|                                                                                                                                                                                     |

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