Programmer´s guide
last change on: 08.11.2019

CAN - EDCP Programmers guide

Description of iseg Enhanced Device Control Protocol to access iseg hardware by CAN bus connection

Document history

Version	Date	Major changes
2.2	08.11.2019	Improve documentation, fixed
2.1	30.08.2017	Revised
2.0	28.1.2016	Relayouted documentation

Disclaimer / Copyright

Important security information

Please read all security warnings and notices carefully. iseg declines responsibility for any kind of damage, injuries or other consequences that are caused by improper use negligence, whether or not under conditional intent.

WARNING!

WARNING!

The non-observance of the advices marked as “Warning!” could lead to possible injury or death.

ATTENTION!

ATTENTION!

Advices marked as “Attention!” describe actions to avoid possible damages to property.

INFORMATION

INFORMATION

Advices marked as “Information” give important information.

Note

The information in this manual is subject to change without notice. We take no responsibility for any errors in the document. We reserve the right to make changes in the product design without notification to the users.

SAFETY ADVICE

WARNING!

WARNING

This device generates high voltages or is part of or attached to high voltage supplying systems.
High voltages are dangerous and may be fatal.

USE CAUTION WHILE WORKING WITH THIS EQUIPMENT.
BE AWARE OF ELECTRICAL HAZARDS.

Always follow at the minimum these provisions:

- High voltages must always be grounded
- Do not touch wiring or connectors without securing
- Never remove covers or equipment
- Always observe humidity conditions
- Service must be done by qualified personnel only

WARNING!

WARNING

RAMP DOWN VOLTAGES !
Before insertion or removal of crate controller, please make sure, all voltages are ramped down, crates are switched off and power cord is disconnected.

ATTENTION!

ATTENTION

CHECK COMPATIBILITY
Please use this device only in compatible MMS crates. Check compatibility list first.

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Kurze Einleitung ähnlich SCPI incl Erklärung der abkürzungen und Co

Die Kapitel 1 und 2 sind nur kopiert (sicherlich falsch inhaltlich) nur zur Anlehnung gedacht.

1 General information to high voltage devices

1.1 Channel and Module

A high voltage channel is a single high voltage output and measurement circuit. The channel has different operation modes and provides different measurements and status flags.

A module is the combination of one or more high voltage channels in a common housing. Examples are a NHS with 6 channels. Beside the combination of all channels, the module provides some more measurement and status information for the whole device.

Module commands set a module-wide function or return a module-wide status or measurement value. Channel commands, in contrast, operate on a specific channel. This channel is specified as command suffix, for example (@1).

1.2 Devices covered by this manual

All devices described in this manual have in common, that they support the EDCP (Enhanced device communication protocol) in combination with the SCPI command set. Some devices also support other command sets, these are not covered by this manual and can be looked up directly in the specific device's manual.

- SHR is a high precision desktop high voltage power supply with four channels of switchable polarity
- NHR is a high precision, high voltage power supply in NIM format, with four channels of switchable polarity
- NHS is a high precision, high voltage power supply in NIM format, with six channels
- MICC is a multipurpose input/output controller to build modular HV systems in 3U MMC format
- EHQ is an one channel high voltage power supply in MME format
- HPS is a series of industrial high voltage devices, typically with one output channel and power greater 300 W
- Filament is a potential-free low voltage power device, typically with one channel and currents starting at 6 A

1.3 High voltage device operation modes

1.3.1 Terminology

Syntax	Declaration
V_{nom}	Voltage nominal, the maximum possible output voltage
I_{nom}	Current nominal, the maximum possible output current
V_{set}	Voltage Set, the user-controllable demanded output voltage
V_{meas}	Voltage Measure, the actual measured output voltage
V_{lim}	Voltage Limit. Can be a hardware or a software limit and serves two purposes: 1. It limits the upper value of V_{set} to the given limit value: $\|V_{set}\| \leq V_{lim}$ 2. It generates the Channel Status is Voltage Limit if V_{meas} exceeds the limit value (the exact threshold value is device dependend)
$I_{set:}$	Current Set, the user-controllable demanded output current
I_{meas}	Current Measure, the actual measured output current
I_{lim}	Current Limit. Can be a hardware or a software limit and serves two purposes: 1. It limits the upper value of I_{set} to the given limit value: $\|I_{set}\| \leq I_{lim}$ 2. It generates the Channel Status is Current Limit if I_{meas} exceeds the limit value (the exact threshold value is device dependend)
V_{bounds}	Voltage bounds, a tolerance tube $V_{set} \pm V_{bounds}$ around V_{set}. If V_{meas} exceeds this tolerance in either direction, the Channel Status is Voltage Bounds is generated. (condition: no ramping)
I_{bounds}	Current bounds, a tolerance tube $I_{set} \pm I_{bounds}$ around I_{set}. If I_{meas} exceeds this tolerance in either direction, the Channel Status is Current Bounds is generated. (condition: no ramping)

1.3.2 Channel operation modes

Operation Mode	Description	
Off	The channel is off, it does not generate high voltage. If all status conditions are satisfied, the channel can be turned on.	
On	The channel is actively generating high voltage.	
Ramping	The channel ramps to the V_{set} if turned on or is turns off with the programmed ramp speed. NHR and SHR devices provide voltage and current ramp speed setting per channel in V/s resp. A/s. All other devices have a common voltage and current ramp speed for all channels in %/s.	
Emergency Off	The channel is shut down without ramp. Afterwards, it stays in Emergency Off until Emergency Clear is given.	
Emergency Clear	The channel leaves the state Emergency Off and goes to state Off. If the channel is not in Emergency Off, nothing happens.	
Kill Enable	The mode Kill Enable provides a higher safety. This mode is module-wide and therefore affects all channels. The channel will got to Trip and shut down without ramp when any of the following conditions occur:	
	• $V_{meas} > V_{lim}$ OR • $V_{meas} > V_{set} + V_{bounds}$ • $I_{meas} > I_{lim}$ OR • $V_{meas} < V_{set} - V_{bounds}$ • $I_{meas} > I_{set}$ OR • $I_{meas} < I_{set} - I_{bounds}$	
Constant Voltage	The channel operates as constant voltage source, that means $V_{meas} \approx V_{set}$ and $I_{meas} < I_{set}$	
Constant Current	The channel operates as constant current source, that meas $V_{meas} < V_{set}$ and $I_{meas} \approx I_{set}$	
Delayed Trip	This is a special mode of Constant Current. If this mode is activated, and I_{meas} reaches or exceeds I_{set}, the Channel Status is Current Trip is generated. Depending on the trip configuration, the channel may stay in Constant Current, or turn off with ramp or shut down without ramp. Trip also happens when Kill Enable is active and any of the Kill conditions occur.	
External Inhibit	External Inhibit is a hardware line to control the high voltage generation. Depending on the device, there might be one External Inhibit per channel or one External Inhibit for all channels. Some devices always shut down the high voltage without ramp on External Inhibit, some devices allow to configure this function.	
	External Inhibit individual per channel	NHS, NHR, SHR
	External Inhibit for all channels	MICC
	External Inhibit is configurable	NHS, NHR, SHR
	External Inhibit shuts down channel without ramp	MICC
Input Error	An input error occurs, if an invalid command or parameter is given, or the parameter of a command exceeds the allowed range. Example: setting a V_{set} of 4000 V for a channel with V_{nom} of 3000 V.	
Output Mode	NHR and SHR devices provide switchable output modes with different voltage and current combinations, e.g. 6 kV/1 mA and 2 kV/3 mA.	
Output Polarity	NHR and SHR devices provide switchable output polarities, positive and negative.	

1.4 Status and Event generation

Channel as well as Module have status and event registers. Both registers contain similar condition bits. The difference between both register types is, that status bits are set and cleared by the device according to the current conditions. Event bits, however, are only set by the device and must be cleared explicitely by the user.

For example, the Status bit is Constant Current indicates that the channel *is now* in constant current mode. The Event bit Event Constant Current in contrast indicates, that the channel has been (or still is) in constant current mode since the last clearing of this bit.

It is thereby possible to clear all status flags at once or to just clear individual bits. In general it is not possible to clear an event bit if the corresponding status bit is still set. The status and event registers are described in detail in section Status and Event registers

2 Introduction to SCPI commands

The high voltage devices can be connected to a control computer by the USB, RS-232, Ethernet, or GPIB interface. All these interfaces use the same general format for commands and query responses. The commands are transmitted as plain text, encoded in the standard 7-bit ASCII character set.

The following special ASCII characters are used in this document:

<CR> (0x0D) the carriage return character

<LF> (0x0A) the line feed character

␣ (0x20) the space character

Two general types of commands exists:

- **Order commands** which have no answer. These always cause the HV device to perform any action. Most often, these commands ends with a parameter that specifies the action. Example: `:VOLT␣ON`
- **Query commands** that returns a response. These generally do not cause the HV device to perform an action other than returning the response. All these commands have a keyword that ends with the "**?**" character. Example: `:MEAS:VOLT?`

2.1 General Command Syntax

Each command is formed by a set of one or more fields. Each field is separated from the next by a field separator. The first field is always the command keyword, the remaining fields and their syntax depend on the command keyword. Commands are always executed in the same order in which they are received. If an error is found in an instruction set, processing of the instruction set is aborted and the remainder of the instruction set is not decoded or executed. For requests containing an error, no answer is sent back.

2.1.1.1 DATA FORMATS

- UI4: An unsigned integer in decimal presentation, with value in the range 0..4294967295. This is the format used for status and event registers.
- Float: A floating point value with the format +1234.567E-6 (sign, mantissa, exponent). This is the format used for voltage and current values.
- String: A character string like "ON" or "OFF". These strings have to be given without quotes (").

3 Crate Controller CC24/23

3.1 Data types

UI1: One byte unsigned integer (8 bit)

CHAR: One ASCII character (8 bit)

UI4: Four byte unsigned integer (32 bit)

R4: Four byte floating point IEEE-754, single precision

All data on the CAN bus is in big endian format, i.e. for UI4 and R4, the highest data byte is transmitted first.

3.2 Access rights

R = Read only: the register can only be read

R/W = Read/write: the register can be read and written

R/C = Read/clear: the register can be read and cleared

3.3 NMT CAN commands (broadcast messages)

The following NMT commands (CAN-ID 0x004) are handled by the Crate Controller:

- NMT_DATAID_START (0xC4)
  - Switches from stop mode to normal operation
  - Message is forwarded to the backplane (and therefore to the modules)
- NMT_DATAID_STOP (0xC8)
  - Switches from normal operation to stop mode to allow the command NMT_RESET_CAN
  - Message is forwarded to the backplane (and therefore to the modules)
- NMT_DATAID_RESET_CAN (0xCC)
  - Re-initializes all CAN interfaces
  - Clears all transmit buffer
  - Clears all statistic registers
  - Message is forwarded to the backplane (and therefore to the modules)
  - Re-initializes the modules CAN interface
  - Modules starts to send their Log-On message

A short delay (10 milliseconds) should be kept between the commands NMT_STOP and NMT_RESET_CAN, so that all messages can be forwarded correctly to the modules.

3.4 Crate Controller commands

3.4.1 Crate Controller Uptime

Crate Controller Uptime	0x1113	UI4	R

This register returns the crate controllers uptime in seconds.

Access	CAN-ID	DLC	DATA_ID	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x1113				
Answer	0x604	6	0x1113	Crate Uptime UI4			

3.4.2 Crate Controller Serial Number

Crate Controller Serial Number	0x1200	UI4	R

This register returns the crate controllers serial number.

Access	CAN-ID	DLC	DATA_ID	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x1200				
Answer	0x604	6	0x1200	Crate Serial Number UI4			

3.4.3 Crate Controller Firmware Release

Crate Controller Firmware Release	0x1201	UI1[4]	R

This register returns the crate controllers firmware release.

Access	CAN-ID	DLC	DATA_ID	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x1201				
Answer	0x604	6	0x1201	Release 1	Release 2	Release 3	Release 4

3.4.4 Crate Controller Firmware Name

Crate Controller Firmware Name	0x1203	CHAR[6]	R

This register returns the crate controllers firmware name.

Access	CAN-ID	DLC	DATA_ID	Data_5	Data_4	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x1203						
Answer	0x604	8	0x1203	'E'	'C'	'H'	'4'	'x'	'A'

3.4.5 Crate Controller Article Description

Crate Controller Article Description	0x1209	CHAR[]	R

This register returns the crate controllers article description. Depending on the length of the article description, multiple CAN messages may be sent. The description is terminated by a zero character.

Access	CAN-ID	DLC	DATA_ID	Data_5	Data_4	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x1209						
Answer	0x604	3...8	0x1209	0	'C'	'C'	'2'	'4'	0

3.4.6 Crate Controller Control

Crate Controller Control	0x1A01	UI4	R/W

The register Crate Controller Control sets crate functions.

Access	CAN-ID	DLC	DATA_ID	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x1A01				
Answer	0x604	6	0x1A01	Crate Control UI4			
Set	0x600	6	0x1A01	Crate Control UI4			

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
res (0)	res (0)	do Set Legacy Mode	set Legacy Mode	do Set Auto Power On	set Auto Power On	do Set Crate Enable Active	set Crate Enable Active
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
res (0)	res (0)	res (0)	res (0)	res (0)	res (0)	res (0)	res (0)
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
res (0)	res (0)	res (0)	res (0)	res (0)	res (0)	res (0)	res (0)
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
res (0)	res (0)	res (0)	res (0)	res (0)	res (0)	do Clear Statistic	do Clear Events

Status Bit	Description
do Clear Events	Clears the crates event status register. This bit can only be written, it always reads zero.
doClear Statistic	Clears the crates statistic registers. This bit can only be written, it always reads zero.
	If this bit is set to one, the high voltage channels can only be turned on, if the pin Crate Enable at the CONTROL connector is pulled high. This bit can only be changed if the backplane is powered off and the bit do Set Crate Enable Active is set to one.
do Set Crate Enable Active	This bit masks the bit set Crate Enable Active. If this bit is zero, the bit set Crate Enable Active is ignored. This bit can only be written, it always reads zero.
set Auto Power On	If this bit is set to one, the backplane is automatically turned on after the mains line is plugged in. Otherwise, the backplane stays off and must be turned on by the POWER ON switch or by remote control. This bit can only be changed if the bit do Set Auto Power On is set to one.
do Set Auto Power On	This bit masks the bit set Auto Power On. If this bit is zero, the bit set Auto Power On is ignored. This bit can only be written, it always reads zero.
set Legacy Mode	If this bit is set to one, the controller operates in Legacy Mode. In this mode, the modules can be controlled by CAN bus connected to CAN1 or CAN2. Note that in this mode, the internal services like isegHAL, iCSservice, SNMP, EPICS can not be used to control the modules. This bit can only be changed if the backplane is powered off and the bit do Set Legacy Mode is set to one.
do Set Legacy Mode	This bit masks the bit set Legacy Mode. If this bit is zero, the bit set Legacy Mode is ignored. This bit can only be written, it always reads zero.

3.4.7 Crate Controller Status

Crate Controller Status	0x1A00	UI4	R

The Crate Controller Status contains the *actual* status. The bits will be set or reset depending on the crates status.

Access	CAN-ID	DLC	DATA_ID	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x1A00				
Answer	0x604	6	0x1A00	Crate Status UI4			

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
res (0)	res (0)	res (0)	res (0)	CAN Bus Error Apalis	CAN Bus Error Backplane	CAN Bus Error CAN1	CAN Bus Error CAN2
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
res (0)	res (0)	Crate Fast Off	Crate Enabled	Shut Down	High Voltage On	Power Fail	Power On
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
res (0)	res (0)	res (0)	Sum Error	High +3.3 CC	Low +3.3 CC	High +5 CC	Low +5 CC
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
High Temperature	Service	High +24 Backplane	Low +24 Backplane	High +5 Backplane	Low +5 Backplane	High +24 Battery	Low +24 Battery

Status Bit	Description
CAN Bus Error Apalis	The internal CAN bus between the Crate Controller and the Apalis is in error state
CAN Bus Error Backplane	The internal CAN bus between the Crate Controller and the HV modules is in error state
CAN Bus Error CAN1	The external CAN bus connected to CAN1 is in error state
CAN Bus Error CAN2	The external CAN bus connected to CAN2 is in error state
High-Voltage-On	Backplane is powered on and at least one channel within the crate has Status.isOn or measured voltage > 63 V The front panel LED HV-ON is derived from this bit.
Power-On	Backplane is powered on (modules are supplied with voltage) The front panel LED Status lights green when Power-On is set and no supply error exists. The front panel LED Status lights red when Power-On is set and a supply error exists.
Power-Fail	AC line power fail detected. Crate without UPS: high voltage is turned fast off Crate with UPS: high voltage is turned off with ramp after the wait time
High Temperature	At least one modules or the crate controller have high temperature. The high voltage is turned off with the configured voltage ramp speed.
Shut Down	If the front button POWER ON is pressed for more than 10 seconds, this bit is set for approx. 1 minute. This is used to perform a shut down of the embedded crate computer.
Sum Error	This bit is set, whenever one of the bits Power Fail, High Temperature, Service, High Supply, Low Supply or Crate Fast Off is set or if Crate Enabled is cleared.
Service	A fatal error occurred. Contact service.
High Supply X	Measured voltage X exceeds the upper limit.
Low Supply X	Measured voltage X exceeds the lower limit.
Crate Enabled	If the crate is enabled, it is possible to turn on high voltage for all channels. The crate is enabled, if the Crate Control bit set Crate Enable Active is not set, or if the CONTROL pin Crate Enable is pulled high.
Crate Fast Off	If the CONTROL pin Crate Fast Off is turned high, the high voltages are shut down without ramp.

3.4.8 Crate Controller Event Status

Crate Controller Event Status	0x1A02	UI4	R/C

The Event Status bits are set together with the status bits. Unlike Status bits, Event Status bits are not reset automatically. The have to be reset by the user, by writing an 1 to this event bit. All Event Status bits are reset by the Crate Control bit do Clear.

Access	CAN-ID	DLC	DATA_ID	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x1A02				
Answer	0x604	6	0x1A02	Crate Event Status UI4			
Clear	0x600	6	0x1A02	Crate Event Status UI4			

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
res (0)	res (0)	res (0)	res (0)	res (0)	res (0)	res (0)	res (0)
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
res (0)	res (0)	res (0)	res (0)	Shut Down	High Voltage On	Power Fail	Power On
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
res (0)	res (0)	res (0)	Sum Error	High +3.3 CC	Low +3.3 CC	High +5 CC	Low +5 CC
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
High Temperature	Service	High +24 Backplane	Low +24 Backplane	High +5 Backplane	Low +5 Backplane	High +24 Battery	Low +24 Battery

3.4.9 Crate Controller Event Mask

Crate Controller Event Mask	0x1A3	UI4	R/W

The Event Mask is defined for compatibility to the module EDCP command set, but not used at the moment.

Access	CAN-ID	DLC	DATA_ID	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x1A03				
Answer	0x604	6	0x1A03	Crate Event Mask UI4			
Set	0x600	6	0x1A03	Crate Event Mask UI4			

3.4.10 Crate Controller Fan Speed Percent

Crate Controller Fan Speed Percent	0x1A04	R4	R

This register returns the crates fan speed in percent (0...100). The fan speed is regulated according to the maximum crate temperature. The maximum temperature is collected over all modules and the crate controller. The maximum fan speed is reached at approx. 45° C.

Access	CAN-ID	DLC	DATA_ID	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x1A04				
Answer	0x604	6	0x1A04	Crate Fan Speed R4			

3.4.11 Crate Power On/Off

Crate Power On/Off	0x1A05	UI1	R/W

This register controls the crates power on (1) or off (0) function.

Access	CAN-ID	DLC	Data_ID	Data_0
Request	0x601	2	0x1A05	
Answer	0x604	3	0x1A05	0x00
Set On	0x600	3	0x1A05	0x01
Set Off	0x600	3	0x1A05	0x00

3.4.12 Crate Chassis Identification

Crate Controller Chassis Identification	0x1A06	UI6	R

This register contains the 1-Wire serial number that is read from the crate chassis. This number is an unique number for every crate. The six bytes are the 1-Wire serial number without manufacturer code and without CRC.

This register is filled once the backplane was turned on for at least ten seconds.

Access	CAN-ID	DLC	DATA_ID	Data_5	Data_4	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x1A06						
Answer	0x604	8	0x1A06	Crate Chassis Identification UI6					

3.4.13 Crate Backplane Type

Crate Backplane Type	0x1A07	UI2	R/C

This register contains the backplane type for the master and all slave crates.

Access	CAN-ID	DLC	DATA_ID	Data_1	Data_0
Request	0x601	2	0x1A07		
Answer	0x604	4	0x1A07	Crate Backplane Type UI2	
Clear	0x600	2	0x1A07		

A write access to this register forces a new scan of the backplane type register. It takes approx. two seconds to scan the system and fill the register again.

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
Reserved	Reserved	Reserved	Green Slave 5	Green Slave 4	Green Slave 3	Green Slave 2	Green Slave 1
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
Reserved	Reserved	Yellow Slave 5	Yellow Slave 4	Yellow Slave 3	Yellow Slave 2	Yellow Slave 1	Master

Bit meaning:

0 = Backplane type iseg: backplane is sequential

1 = Backplane type wiener: backplane is not sequential

Bit position:

0 = Master crate

1...5 = Slave crates on CAN line yellow (1 = Slave 0, 2 = Slave 1, ...)

8...12 = Slave crates on CAN line green (8 = Slave 0, 9 = Slave 1, ...)

3.4.14 Crate Temperature Sensor

Crate Temperature Sensor	0x2001	R4	R

This register contains the actual temperature for different sensors.

Sensor 0 and 1 are placed at the crate controller. Sensor 2 is the maximum temperature in the crate (collected over all modules and the crate controller). The maximum temperature is used to control the crates fan speeds.

If the request is done with DLC = 2, all temperature sensors are returned in three CAN messages. If the request is done with DLC = 3 and a specific sensor, only this sensor is returned.

Access	CAN-ID	DLC	DATA_ID	Sensor	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x2001					
Answer	0x604	7	0x2001	0x00	Crate Temperature 0 R4			
	0x604	7	0x2001	0x01	Crate Temperature 1 R4			
	0x604	7	0x2001	0x02	Crate Temperature 2 R4			
Request	0x601	3	0x2001	0x01				
Answer	0x604	7	0x2001	0x01	Crate Temperature 0 R4			

3.4.15 Crate Supply Measurement

Crate Supply Measurement	0x2002	R4	R

This register contains the measured supply voltages.

If the request is done with DLC = 2, all supply measurement values are returned in consecutive CAN messages. If the request is done with DLC = 3 and a specific supply number, only this measurement value is returned.

Access	CAN-ID	DLC	DATA_ID	Supply	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x2002					
Answer	0x604	7	0x2002	0x00	Crate Supply Measurement 0 R4			
	0x604	7	0x2002	0x01	...			
	0x604	7	0x2002	0x08	Crate Supply Measurement 8 R4			

3.4.16 Crate Supply Nominal

Crate Supply Nominal	0x2003	R4	R

This register contains the nominal supply voltages.

If the request is done with DLC = 2, all supply nominal values are returned in consecutive CAN messages. If the request is done with DLC = 3 and a specific supply number, only this nominal value is returned.

Access	CAN-ID	DLC	DATA_ID	Supply	Data_3	Data_2	Data_1	Data_0
Request	0x601	2	0x2003					
Answer	0x604	7	0x2003	0x00	Crate Supply Nominal 0 R4			
	0x604	7	0x2003	0x01	...			
	0x604	7	0x2003	0x08	Crate Supply Nominal 8 R4			

3.5 Statistic registers

For each CAN bus, multiple statistic registers are kept. The Crate Controller owns four CAN busses, which are numbered the following way:

0) CAN PC
1) CAN Backplane
2) CAN 2
3) CAN 1

The existing statistic registers are described below.

If a request message without a CAN bus number (DLC = 2) is received, the statistic register for all four CAN busses are returned.

The statistic counter are incremented by the crate controller and can be reset by the NMT command NMT_CAN_RESET together with the CAN interfaces or by the Crate Control bit do Clear Statistic.

3.5.1 CAN Bus Received

CAN Bus Received	0x2040	UI4	R

This register counts the received messages for the given CAN bus.

Access	CAN-ID	DLC	DATA_ID	CAN bus	Data_3	Data_2	Data_1	Data_0
Request	0x601	3	0x2040	00				
Answer	0x604	7	0x2040	00	Received Messages UI4			

3.5.2 CAN Bus Receiver Overrun

CAN Bus Receiver Overrun	0x2041	UI4	R

This register counts the receive buffer overruns for the given CAN bus. A receive buffer overrun occurs, if a CAN message could not be read in time from the CAN bus.

This register should always be zero.

Access	CAN-ID	DLC	DATA_ID	CAN bus	Data_3	Data_2	Data_1	Data_0
Request	0x601	3	0x2041	00				
Answer	0x604	7	0x2041	00	Receiver Overrun Messages UI4			

3.5.3 CAN Bus Transmitted

CAN Bus Transmitted	0x2042	UI4	R

This register counts the transmitted messages for the given CAN bus.

Access	CAN-ID	DLC	DATA_ID	CAN bus	Data_3	Data_2	Data_1	Data_0
Request	0x601	3	0x2042	00				
Answer	0x604	7	0x2042	00	Transmitted Messages UI4			

3.5.4 CAN Bus Transmit Buffer Full

CAN Bus Transmit Buffer Full 0x2043 UI4 R

This register counts the messages, that could not be sent to the given CAN bus because of full transmit buffer.

Access	CAN-ID	DLC	DATA_ID	CAN bus	Data_3	Data_2	Data_1	Data_0
Request	0x601	3	0x2043	00				
Answer	0x604	7	0x2043	00	Transmit Buffer Full UI4			

3.5.5 CAN Bus Dropped

CAN Bus Dropped 0x2044 UI4 R

This register counts the messages that were received from the given CAN bus and could not be routed because of unclear destination.

This register should always be zero.

Access	CAN-ID	DLC	DATA_ID	CAN bus	Data_3	Data_2	Data_1	Data_0
Request	0x601	3	0x2044	00				
Answer	0x604	7	0x2044	00	Dropped Messages UI4			

3.5.6 CAN Bus Error

CAN Bus Error 0x2045 UI4 R

This register is incremented every second when the given CAN bus is in error state.

Access	CAN-ID	DLC	DATA_ID	CAN bus	Data_3	Data_2	Data_1	Data_0
Request	0x601	3	0x2045	00				
Answer	0x604	7	0x2045	00	Error Seconds UI4			

3.5.7 CAN Bus Throttle

CAN Bus Throttle 0x2046 UI4 R

This register counts the number of generated throttle messages for the given CAN bus.

Access	CAN-ID	DLC	DATA_ID	CAN bus	Data_3	Data_2	Data_1	Data_0
Request	0x601	3	0x2046	00				
Answer	0x604	7	0x2046	00	Throttle Messages UI4			

3.5.8 CAN Bus Status

CAN Bus Status	0x2047	UI4	R

This register holds the current status for the given CAN bus.

Access	CAN-ID	DLC	DATA_ID	CAN bus	Data_3	Data_2	Data_1	Data_0
Request	0x601	3	0x2047	00	1	2	3	4
Answer	0x604	7	0x2047	00	Bus Status UI4			

The CAN Bus Status register contains the following information:

- Receiver bus status: Ok (0), Warning (1), Error (2), Bus off (3)
- Transmitter bus status: Ok (0), Warning (1), Error (2), Bus off (3)
- CAN hardware activated
- CAN hardware synchronized with CAN bus
- CAN hardware in special mode (initializing, sleep, listen-only, loopback).
  These bits should not be set in normal operation conditions.

The CAN hardware status is refreshed at the time of the request.

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
		Loopback	Listen Only	Enabled	Synchronized	Sleeping	Initializing
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
Transmitter bus status (0 = Ok, 1 = Warning, 2 = Error, 3 = Bus off)							
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
Receiver bus status (0 = Ok, 1 = Warning, 2 = Error, 3 = Bus off)							

3.5.9 CAN Bus Disabled

CAN Bus Disabled	0x2048	UI4	R

This register counts the number of dropped messages because the given CAN bus is not enabled (e.g. backplane is off).

Access	CAN-ID	DLC	DATA_ID	CAN bus	Data_3	Data_2	Data_1	Data_0
Request	0x601	3	0x2048	00				
Answer	0x604	7	0x2048	00	Disabled Messages UI4			

3.5.10 CAN Bus Bitrate

CAN Bus Bitrate	0x2049	UI4	R

This register holds the current bit rate for the given CAN bus.

Access	CAN-ID	DLC	DATA_ID	CAN bus	Data_3	Data_2	Data_1	Data_0
Request	0x601	3	0x2049	00				
Answer	0x604	7	0x2049	00	Bitrate UI4			

3.6 Examples

CC = Crate-Controller, PC = Controlling PC

Message	Direction	CAN-ID	DLC	Data ID	Data	Data	Data	Data
Log-On Request	CC → PC	601	3	D8 00	2E			
Log-On Confirmation	CC → PC	600	2	D8 01				
Status Request	PC → CC	601	2	1A 00				
Status Answer	CC → PC	604	6	1A 00	00	00	00	00
Crate Power On	PC → CC	600	3	1A 05	01			
Crate Power Off	PC → CC	600	3	1A 05	00			
Fan Speed Request	PC → CC	601	2	1A 04				
Fan Speed Answer	CC → PC	604	6	1A 04	40	A0	00	00

Request Temperatures and Supplies (group request)

Message	CAN-ID	DLC	DataID	Channel	Data	Data	Data	Data	Value
Request all Temperatures	601	2	20 01						
Temperature 0	604	7	20 01	00	41	EF	0D	B0	29.9 °C
Temperature 1	604	7	20 01	01	41	ED	66	30	29.7 °C
Temperature 2	604	7	20 01	02	41	EF	0D	B0	29.9 °C
Request all Measured Supplies	601	2	20 02						
Backplane +24	604	7	20 02	00	41	BE	75	98	23,8 V
Reserved	604	7	20 02	01	00	00	00	00	0 (res)
Backplane +5	604	7	20 02	02	40	A0	51	EC	5,01 V
Reserved	604	7	20 02	03	00	00	00	00	0 (res)
Reserved	604	7	20 02	04	00	00	00	00	0 (res)
Supply +5	604	7	20 02	05	40	9F	A2	1B	4,99 V
Supply +3.3	604	7	20 02	06	40	53	2E	1C	2,99 V
Reserved	604	7	20 02	07	00	00	00	00	0 (res)
Battery + 24	604	7	20 02	08	41	D0	CC	CD	26,1 V

4 EDCP CAN for High Voltage Devices

4.1 General information

Each single HV channel is independently controllable. The units are software controlled via CAN-Interface through a PC or similar controller.

Using an iseg crate combined with a CC24 controller or an iCSmini as stand alone iseg communication server WEB-services, Remote-service, EPICS and SNMP are possible via Ethernet.

We offer a comfortable control program “isegCANHVControl” for up to 64 iseg modules with CAN interface under Windows and „iseg OPC Control“ in connection with the „iseg OPC Server”.

Using the w-ie-ner Mpod crate it is possible to control up to 10 modules via Ethernet-SNMP Interface.

4.2 General settings and options

Please note that there are additional hardware features for these devices in this manual called **OPTION**. The use of an access without the hardware implementation will be described under **OPTION** in manual.

Devices with different bit rate settings do not work on the same CAN bus.

The actual channel and module values (measurement and status) are refreshed approximately every 10ms x number of channels.

The board temperature values are refreshed approximately every 5 up to10 s.

5 Operation principle

5.1 Remote interface control

The Multi-Channel HV modules are controlled via a remote interface. The communication between an application and the module is performed by the transmission of data items. A data item contains information to be submitted to and/or received from the module. It can represent a specific quantity or a union of single bits. The majority of the data items are standard for all Multi-Channel HV modules and are described in the interface manual in detail. Data items for optional functions are described in the interface options manual.

A general distinction can be made between data items to control individual HV channels and data items to control the HV modules with the sum of all contained channels.

The former group includes the following data items, which exist for every single HV channel:

- items to handle channel status, control and event's
- items to set the voltage or current, bounds, interlock maximum and minimum
- items to read the measured voltage and current
- items to read the nominal voltage and current

The following data items control the properties of the whole HV module. These items exist only once per module:

- items to handle module status, control and events
- voltage ramp speed (is the same for all HV channels)
- current ramp speed (is the same for all HV channels)
- restart time after recalling set values
- maximum set voltage
- maximum set current
- ADC samples per second
- digital filter setting
- power supply voltages
- temperature
- maximum voltage
- maximum current

5.1.1 Operation modes

There are three operation modes depending on the HV hardware and the module configuration.

5.1.2 Constant Voltage (CV)

In the mode Constant Voltage the module works as a constant voltage source. For this mode it is required that the value for current set (Iset) or current trip (Itrip) is greater than the resulting output current.

5.1.3 Constant Current (CC)

In the mode Constant Current the module works as a constant current source. For this mode it is required that the HV channel has implemented a current control and that the current set value Iset is smaller than the current that would result from set voltage and the load at the HV output.

5.1.4 Current trip

This is a special case of the Constant Voltage mode. The module usually provides a constant output voltage, where the value of the parameter Itrip defines a current limit. If this value is reached or exceeded (e.g. by arcs), in this mode the channel will be switched off immediately.

5.1.5 Function KillEnable

KillEnable is a global control signal that defines the behaviour of the module if a given voltage (Vmax) or current limit (Imax/Iset/Itrip) is exceeded.

If KillEnable is active the violation of one of the limits will trigger a Kill-signal in the respective channel. This signal will switch off the channel immediately without ramp.

If KillEnable is inactive and one of the limits Imax/Iset or Itrip is exceeded the following will happen:

- HV hardware with current control - switch the channel from voltage control into current control.
- HV hardware without current control – a trip in the channel hardware will switch off the high voltage generation. Then the module automatically starts to restore the HV via a voltage ramp to the set voltage. If the HV is held during the trip, e.g. by an external capacity load, the recovery of the HV starts from the voltage at the output. The auto-recovery of the voltage is performed only once in a time span of 10 minutes. If the channel trips a second time within the 10 minutes the HV will be switched off.

5.1.6 Additional current measuring range (Option)

Some modules are equipped with a second current measuring range to capture small current values. The range is automatically detected. In the second range the values will be converted with a higher resolution. The value is in the same floating point format as in the first range. The device control protocol allows to request which range is active.

INFORMATION

NOTE

The second range cannot be activated if:

- function KillEnable is on.
- a voltage ramp up is running.
- the module operates in CC mode.

5.2 Control and Status items

5.2.1 Controls

Control items encapsulate a number of bits which allow to switch On or Off specific functions. There is a control item for the module (ModuleControl) and one for each channel (ChannelControl). Control bits that are used to switch a function permanently are named “set…” (e.g. “setON” to switch a channel On of Off). Bits that initiate the execution of a task just once are named “do…” (e.g. “doClear” to clear all events).

5.2.2 Status and events

Status items contain a register that encapsulates bits that indicate the current status of the module or channel. Status bits are named starting with “is…”. The status always displays only present conditions, if a condition has changed corresponding status bits will be updated.

Unlike the status, event items record previous conditions (e.g. exceeded limits, trips etc.). If an event is registered the corresponding event bit is set permanently to “1” and will keep the information until explicitly reset. Event bits are named starting with “E…”.

status Summary of actual condition of module, channel or group

event Event, characterizes a former or actual special condition of module, channel or group

5.2.3 Event status and event mask

To avoid the need for checking all event sources permanently for incoming events, the module provides a hierarchical chain for the combination of the events to a single status bit. The structure for the event processing allows a combination of events coming from the module status, the status of the channels and the group status. For each event status item a corresponding event mask item is provided. The event mask defines which event status bits contribute to the combined event status.

Event status Events that have been registered so far

Event mask Filter to define which individual events contribute to the summarized event

Between event status items and the corresponding mask is a bit by bit correspondence. The bits in the mask are named starting with “ME…”. If the mask bit is set, the occurring of the respective event will activate the combined event. In turn these sum events are collected in an event status register and connected with an event mask register at this higher level.

CAUTION!

CAUTION!

If an event bit in the EventStatus is active and the corresponding bit in the EventMask is set, it is not possible to ramp up the voltage or to activate the HV generation if it has been switched off. To unblock this the EventStatus bits must be reset by writing “1” on the corresponding bit positions.

Individual events in the channel event status are starting point of the event combination logic.
First each event status bit for the channel is combined with the corresponding bit in the event mask using a logical AND. Then an event status bit for the channel is generated by combining all resulting bits with a logical OR. The full logical operation is given by

EventChannelStatus[n] = (Channel[n].EventVoltageLimit AND Channel[n].MaskEventVoltageLimit) OR
(Channel[n].EventCurrentLimit AND Channel[n].MaskEventCurrentLimit) OR
(Channel[n].EventCurrentTrip AND Channel[n].MaskEventCurrentTrip) OR
(Channel[n].EventExtInhibit AND Channel[n].MaskEventExtInhibit) OR
(Channel[n].EventVoltageBounds AND Channel[n].MaskEventVoltageBounds) OR
(Channel[n].EventCurrentBounds AND Channel[n].MaskEventCurrentBounds) OR
(Channel[n].EventControlledVoltage AND Channel[n].MaskEventControlledVoltage) OR
(Channel[n].EventControlledCurrent AND Channel[n].MaskEventControlledCurrent) OR
(Channel[n].EventEmergency AND Channel[n].MaskEventEmergency) OR
(Channel[n].EventEndOfRamp AND Channel[n].MaskEventEndOfRamp) OR
(Channel[n].EventOnToOff AND Channel[n].MaskEventOnToOff) OR
(Channel[n].EventInputError AND Channel[n].MaskEventInputError)

The result of the first step for all channels is stored in the register EventChannelStatus.
In the next step all bits of the EventChannelStatus are combined to a single status bit, using the corresponding mask (EventChannelMask). The logical operation is given by

EventChannelActive = (EventChannelStatus[0] AND EventChannelMask[0]) OR
(EventChannelStatus[1] AND EventChannelMask[1]) OR
...
(EventChannelStatus[n] AND EventChannelMask[n])

A second branch in the event processing logic treats events generated by the status of the module. The following scheme applies to these module events:

EventModuleActive = (EventTemperatureNotGood AND MaskEventTemperatureNotGood) OR
(EventSupplyNotGood AND MaskEventSupplyNotGood) OR
(EventSafetyLoopNotGood AND MaskEventSafetyLoopNotGood)

A third branch combines events generated by groups (monitor group, timeout group, see chapter 3)
Group events are stored in the status register EventGroupStatus. The mask EventGroupMask is used to generate the combined bit EventGroupActive with the following operation:

EventGroupActive = (EventGroupStatus[0] AND EventGroupMask[0]) OR
(EventGroupStatus[1] AND EventGroupMask[1]) OR
...
(EventGroupStatus[32] AND EventGroupMask[32])

Finally the three branches are combined to the bit IsEventActive in the register ModuleStatus:

IsEventActive = EventChannelActive OR EventModuleActive OR EventGroupActive

5.3 Summarizing channel characteristics into groups

The module provides a highly flexible group functionality. A group is a combination of all or a selection of channels with the ability to control or monitor a specified quantity or characteristic of all included channels. There are two classes of groups “Fix Groups” and “Variable Groups”. The former are predefined groups that allow to set single specification values in all channels.

The latter are configurable groups that allow to customize the logical structure of the module to the logical structure of the application. They allow an arbitrary assignment of channels and provide a wide range of functionality, structured in four predefined group types. Up to 32 Variable Groups can be defined. The predefined group types are:

5.3.1 Set Group

sets a specified channel characteristic in all selected channels

no event generation

5.3.2 Status Group

represents the status (condition) of a channel characteristic for all channels

no event generation

5.3.3 Monitor Group

monitors the condition of a channel characteristic for selected channels

event generation when the condition changes

configurable response (e.g. switch off)

5.3.4 Timeout Group

monitors the current trip in selected channels

to employ this group the signal KillEnable must be turned off

Event generation only after expiry of a predefined time within which the trip condition must be active

configurable response (e.g. switch off)

5.3.5 Responses on events (Soft-Kill features)

Event generating groups can be configured to perform one out of four predefined responses if the event has been generated:

- shut down of the whole module without ramp
  - high voltage in all channels of the module is switched off
- switch off all channels that are members of the group without ramp
  - high voltage in all channels of the group is switched off
- switch off all channels that are members of the group with ramp
  - high voltage in all channels of the group is ramped down
- no response
  - no change

6 Communication via Interface

All modules are controlled via a serial CAN bus interface according to CAN bus specification 2.0A. The actual control protocol is the "Enhanced Device Control Protocol" and is explained more precisely in the following sections.

Furthermore it is implemented a second command set, which corresponds to the older standard protocol "Device Control Protocol". The description of the Device Control Protocol is carried out in the corresponding manual.

6.1 Enhanced Device Control Protocol EDCP

The communication between the controller and the module is working according to the Enhanced Device Control Protocol EDCP, which has been designed for instruments of Multi-Channel systems by iseg Spezialelektronik GmbH. This protocol is working according to the master slave principle. Therefore, the control of the HV device through a controller in the superior layer is the master in this system, while the module (as a Front-end device with intelligence) is the slave.

The data exchange between the controller and the HV device is working with help of data frames. These data frames are made out of one direction bit DATA_DIR, one 16bit DATA_ID and further data bytes. The direction bit DATA_DIR defines whether the data frame is a write or read-write access. Write access means that the host writes data into the module, read-write access means that the host wants to read data from the module (this is the read access), and the module answers by a write access.

The DATA_ID is characterized through the first bit of the data frame with DATA_ID.b15=0 of EDCP frames (DATA_ID.bit7=1 of standard DCP frames). In order to code the type of an access the bit14=1 for a **single channel** access (symbol **S**), b13=1 for a **group access** (symbol **G**) and b12=1 for a **module access** (symbol **M**).

The next tables will give an overview of the parts of the EDCP:

Access	DATA DIR	DATA_ID bits								CHN bits	
		Bit15	Bit14	Bit13	Bit12	...	...	Bit1	Bit0	Bit7...	... Bit0
Enhanced DATA_ID	1/0	0	S	G	M	x	x	x	x		
Single channel CHN Write access	0	0	1	0	0	S11	...	S1	S0	C7	C0
Single channel CHN Read-write access	1/0	0	1	0	0	S11	...	S1	S0	C7	C0
Module Write access	0	0	0	0	1	M11	...	M1	M0		
Module Read-write access	1/0	0	0	0	1	M11	...	M1	M0		
Notes: x - any											

If the type of the data frame is a single channel access it will code the corresponding channel information with help of the next multiplex of channel byte (symbol CHN). If the type of the data frame is a module access then a DATA_ID is necessary only.

Access	DATA DIR	DATA_ID bits								CHN / MBR bits		OFFSET
		Bit15	Bit14	Bit13	Bit12	...	...	Bit1	Bit0	Nmax	Nmin	
Enhanced DATA_ID	1/0	0	S	G	M	X	X	X	X			
Single channel CHN of members MBR	1	0	1	1	0	S11	...	S1	S0	M15 to M0 (MBR)		0, 16 ,32
Replay	0									C7 to C0 (CHN)		
Notes: x - any												

If the type of the data frame is a single channel and group access then it will code the corresponding channel members with help of the next 16bit word (symbol MBR, channel15=bit15, .. , channel0=bit0) followed by an OFFSET byte to have a channel start index in steps of 16. If a HV device has received such a request message it will answer with multiple CAN frames for all channels which are addressed as members (MBR).

NOTE MBR=0 will address all channels of the module!

Access	DATA DIR	DATA_ID bits						CHN / NBR bits			OFFSET
		Bit15	Bit14	Bit13	Bit12	...	Bit0	Bit7	....	Bit0	
Group of members MBR Write access	0	0	S	G	M	X	X	N7	.... NBR	N0	
Group of members MBR Read-write access	1 0	0	0	1	0	G11	G0	Ch7 C7	.... CHN	C0 C0	M15 ... M0 (MBR) 0, 16 ,32

If the type of the data frame is a group access than it will coded the corresponding group number symbol NBR, the channel members symbol MBR and the channel start index symbol OFFSET.

These data frames correspond to a transfer into layer 3 (Network Layer) and layer 4 (Transport Layer) of the OSI model of ISO. The transmission medium is the CAN Bus according to specification 2.0A, related to level1 (Physical Layer) and level 2 (Data Link Layer).

The Enhanced Device Control Protocol EDCP has been matched to the CAN Bus according to specification CAN 2.0A. Therefore specials of layer 1 and 2 are mentioned only if absolutely necessary and if misunderstandings of functions between the Transport Layer and functions of the Data Link Layer may be possible. The communication between the controller and a module on the same bus segment can be described as follows.

6.2 CAN-Bus Implementation

The data frame structure is matched to the message frame of the standard-format according to CAN specification 2.0A, whereas looking from the point of view of the CAN protocol a pure data transmission will be done, which is not applying to the protocol.

The data frame of the EDCP will be transferred as data word with n bytes length in the data field of the CAN frame according to the specific demand of the related access. Therefore this results into a Data Length Code (DLC) of the CAN-protocol of n.

It is possible to transfer 8 data bytes that apply to the DLC field with decreasing values.

The addressing of the Front-end device is also made using the 11 bit identifier of the CAN protocol.

In order to keep the CAN segment open also for other protocols, the address room has been limited to 64 nodes.

ID10 is dominant.

ID9 When the Event structure of the module was configured and the bit isEvntActive in the ModuleStatus was triggered, then the module will send the DCP Module frame General status as an active message with higher priority (ID9 = 0) than normal messages.

ID8 to ID3
allow the addressing of 64 Front-end devices (ID3: A0 = 20 ;...; ID8: A5 = 25), see 3.2 Back Panel also.

ID2 is used for a special network management service (NMT).

ID1 is not used.

ID0 is used for defining the direction of the data transfer (DATA_DIR). The controller therefore will start a read-write access for data with DATA_DIR = 1 and will send data with DATA_DIR=0. The Front-end device responds to the data request by sending the corresponding data with DATA_DIR = 0.

That means all “even” CAN-ports (Identifier) are interpreted as ‘Write ports’ all “odd” CAN ports as ‘ Read ports’.

Only if the Front-end device is not registered at the controller or if it does not receive valid data during a longer time period (ca. 1 min), then it will actively send the registration frame with DATA_DIR = 1 (see also item 4.3). The RTR Bit is always set to zero.

In one CAN segment modules with unequal identifier and equal bit rate are allowed only. The factory fixed bit rate is written on the sticker of the 96-pin connector.

Data formats:

The data format on the network is big endian, i.e. on Intel computers, the value is stored byte-wise reverse. To convert floating-point values to their hexadecimal representation, the online calculator http://babbage.cs.qc.edu/IEEE-754/ can be used. Nur SuchLink anbieten (https://www.google.de/search?ei=KqaxXceRBI3osAeoqbaoDg&q=little+big+endian+converter+online&oq=big+endian&gs_l=psy-ab.1.0.0i71l8.0.0..3594...0.2..0.0.0.....0.....gws-wiz.OF9wdv62Vg0)

UI1	unsigned character
SI1	signed character
UI2	unsigned short integer (16 bit)
UI4	unsigned integer (32 bit)
R4	float according to IEEE-754 single precision format

Example Vset = 1000 V:

Data-Bytes on the network – 0x44 0x7a 0x00 0x00

Data-Bytes in computers using a little endian memory – 0x00 0x00 0x7a 0x44

Conventional CAN data frame to control of the HV modules, see ehq_multi_channel_can also.

CAN data frame to control the HV modules

S	Identifier	R			DLC	n – data bytes (1 to 8)					CRC	ack
O		T	0	0	(n=1-8)	DATA_ID Single channel access	CHN	DATA_(n-3) 0	DATA_(n-4) 0	DATA_ …		F.
F	b10 … b0	R	Reserve		b3 b0	b15=0 1 0 0 b0	C7 C0	b7 b0	b7 b0	b7 b0	15 bit	

S	Identifier	R			DLC	n – data bytes (1 to 8)					CRC	ack
O		T	0	0	(n=1-8)	DATA_ID Multiple single channels access	MBR	DATA_(n-4) 0	DATA_(n-5) 0	DATA_ …		F.
F	b10 … b0=1	R	Reserve		b3 b0	b15=0 1 1 0 b0	M15 M0	b7 b0	b7 b0	b7 b0	15 bit	

S	Identifier	R			DLC	n – data bytes (1 to 8)					CRC	ack
O		T	0	0	(n=1-8)	DATA_ID Group access	NBR	OFFSET	ChList	Type …		F.
F	b10 … b0	R	Reserve		b3 b0	b15=0 0 1 0 b0	N7 N0	b7 b0	b15 b0	b15 b0	15 bit	

S	Identifier	R			DLC	n – data bytes (1 to 8)				CRC	ack
O		T	0	0	(n=1-8)	DATA_ID Module access	DATA_(n-2) 0	DATA_(n-3) 0	DATA_ …		F
F	b10 … b0	R	Reserve		b3 b0	b15=0 0 0 1 b0	b7 b0	b7 b0	b7 b0	15bit	

ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	0	0	0	0	0	0	0	1	0	DATA_DIR

1. Acceptance-Filter of the CAN-Controller is set to NMT service identifier

ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	P	A5	A4	A3	A2	A1	A0	0	0	DATA_DIR

2. Acceptance-Filter of the CAN-Controller is set to FE-address A0 - A5

The Front-end device must do:

- Processing of NMT services via broadcast messages inside of the CAN segment
- Processing of the single accesses with direct channel values.
- Processing of group information of the module.
- Self-registration in the higher level through sending the module address.
- Building of status information.
- Send an active error message with higher priority if one of the bits - sum status, supply voltages or safety loop - in the group access “General status module” not has been set (the module must be configured as a CAN-node with an Active-CAN message function).

6.3 Summary of CAN data frame accesses via the NMT service identifier

Access	DATA_DIR	BYTE	NMT DATA_ID Bit								read / write / active	DATA-Bytes	Page
	ID0	hex	7	6	5	4	3	2	1	0			
No NMT DATA_ID	x		0	x	x	x	x	x	x	x			
NMT service CAN segment	0		1	1	N3	N2	N1	N0	R1	R0			
NMT Address (MICC only)	0/1	0x30	0	0	1	1	0	0	0	0	w	0/2/3	
NMT Start	0		1	1	0	0	0	1	x	x	w	1	18
NMT Stop	0		1	1	0	0	1	0	x	x	w	1	18
NMT Reset CAN	0		1	1	0	0	1	1	x	x	w	1	18
NMT Reset hardware	0		1	1	0	1	0	0	x	x	w	1	18
NMT set of Bit rate	0		1	1	0	1	0	1	x	x	w	3	18
NMT temperature set	0		1	1	0	1	1	0	x	x	w	3	19
NMT mode set	0		1	1	1	0	0	0	x	x	w	2/6	19
NMT set standard DCP or enhanced DCP	0		1	1	1	0	0	1	x	x	w	2	19
NMT channel group set	0		1	1	1	0	1	0	x	x	w	8/6	19
NMT module set	0		1	1	1	0	1	1	x	x	w	8/6	19
N3..N0: NMT access													
R1..R0: reserved													

NMT Address (MICC only)

Access	CAN ID (NMT)	RTR	EXT_INSTR	DATA_DIR	DATA_ID	DATA_1	DATA_0
NMT-RTR master	0x004	1	0	0	-	-	-
NMT-RTR board reply	0x003	0	0	0	0xC0	address	-
NMT Addess master write	0x004	0	0	0	0xC0	old address	new address

NMT Start	The state of all Front-end devices is going to OPERATIONAL (see Appendix C) Link falsch!
NMT Stop	The state of all Front-end devices is going to PREPARED This is necessary before storing any information permanently in EEPROM or execute one of the following NMT services.
NMT Reset CAN	re - initialise all connected iseg Multi-Channel CAN devices.
NMT Reset hardware	execute a hardware reset of all connected CAN devices.
NMT set of Bit rate	set a new bit rate for all connected iseg Multi-Channel CAN devices (DATA_1 / DATA_0 see group access Bit rate)
NMT set of temperature	An offset for the calculation of the temperature will be calculated in all modules which receive this message.
all devices DATA_1 to DATA_0	measured temperature in tenth parts of °C UI2

DATA_1	DATA_0
MSB	LSB

NMT mode (stand im 2017 Dokument über der Tabelle)

Mode	Data_0	Description
NORMAL_MODE	000	Operating Mode “Operational" without any condition
FACTORY MODES	001 - 005	will used in production of the modules only!
LIVE_INSERTION_MODE	006	Mode to avoid events during a live insertion

NMT set standard DCP or enhanced DCP: DATA_0=0 standard DCP DCP

DATA_0=1 enhanced DCP EDCP

NMT broadcast messages (ANORDNUNG??) Hintergrund?

NMT channel group set frame:

Access	DATA_DIR	NMT DATA_ID	GROUP	EDCP DATA_IDEDCP Multiple Single Channels Access	DATAn	DATAn-1	DATAn-2	DATAn-3
NMT group voltage set	0	0xe8	Group	0x6100	Voltage [R4]			
NMT group current set	0	0xe8	Group	0x6101	Current [R4]			
NMT group control set	0	0xe8	Group	0x6001	Control [UI2]			
NMT group event mask set	0	0xe8	Group	0x6003	Event mask [UI2]			

Group 0..255 (group = 0 after power on of the module)

NMT module set frame:

Access	DATA_DIR	NMT DATA_ID	GROUP	EDCP DATA_ID EDCP Module Access	DATAn
NMT voltage ramp speed set	0	0xec	reserved	0x1100	Voltage ramp speed [R4]
NMT current ramp speed set	0	0xec	reserved	0x1101	Current ramp speed [R4]
NMT control set	0	0xec	reserved	0x1001	Control [UI2]
NMT event mask	0	0xec	reserved	0x1003	Event mask [UI2]
NMT event channel mask	0	0xec	reserved	0x1005	Event mask [UI2]

With one of the NMT channel group set or the NMT module set frames a message is sent to the corresponding data point of the table above in kind of a broadcast information for all channels, which have the same group number GROUP. The detailed description of the frames can be found by a click on the arrows of the tables. The EDCP Single Channel Access GroupNumber (described on page 30) handles the distribution of a group number for each channel.

The NMT channel group set and NMT module set frames has been implemented since following firmware releases:

Name of firmware	Firmware release	Device class
E16D0	00.04.02.01	21
E16D1	00.04.02.01	21
E08C0	00.02.02.00	24
E16C1	00.01.00.00	70
E08C2	00.01.00.00	27
E08F0	00.02.02.08	25
E08F2	00.04.00.06	26

IST DIE TABELLE NOCH AKTUELL?

Example: Switch ON all channels of the whole system (group number after reset of all channels is zero)

ID	DLC	NMT DATA_ID	GROUP	EDCP DATA_ID Multiple Single Channel Access	Channel control
0x004	0x6	0xe6	0x00	0x6001	0x0008

6.4 Summary of CAN data frame accesses via the Front-end-address identifier

Multi-channel High Voltage CAN modules are made out of one or two PCBs (in order to double the number of HV channels) and one digital CAN Interface per PCB.

Each module board has to be controlled separately via its own CAN nodes identifier (see chapter above).

6.4.1 List to access of the EDCP made for HV boards up to 255 channels EDCP Single Channel Accesses

Access	DATA_DIR	WORD	DATA_ID Bit									read / write / active	DATA-Bytes	Page
	ID0	hex	15	14	13	12	11	...	...	1	0			
DATA_ID			0	S	G	M	x [2]	x [2]	x [2]	x [2]	x [2]			
Single channel access	**1/0**	**0x4xxx**	**0**	**1**	**0**	**0**	**S11 ... S0** [1]							
ChannelStatus	1	0x4000	0	1	0	0						r	3/5	45
ChannelControl	0/1	0x4001	0	1	0	0			0x001			w/r	3/5	47
ChannelEventStatus	1/0	0x4002	0	1	0	0			0x002			r/w	3/5	48
ChannelEventMask	0/1	0x4003	0	1	0	0			0x003			w/r	3/5	50
DelayedTripAction	0/1	0x4006	0	1	0	0			0x006			w/r	3/4	51
DelayedTripTime	0/1	0x4005	0	1	0	0			0x005			w/r	3/5	52
ExternalInhibitAction	0/1	0x4007	0	1	0	0			0x007			w/r	3/4	53
VoltageSet	0/1	0x4100	0	1	0	0						w/r	3/7	54
CurrentSet / CurrentTrip	0/1	0x4101	0	1	0	0						w/r	3/7	54
VoltageMeasure	1	0x4102	0	1	0	0						r	3/7	55
CurrentMeasure	1	0x4103	0	1	0	0						r	3/7	55
VoltageBounds	0/1	0x4104	0	1	0	0						w/r	3/7	56
CurrentBounds	0/1	0x4105	0	1	0	0						w/r	3/7	56
VoltageNominal	1	0x4106	0	1	0	0						r	3/7	57
CurrentNominal	1	0x4107	0	1	0	0						r	3/7	57
CurrentMeasure Range	1	0x4109	0	1	0	0						r	3/8	57
VctCoefficient	1/0	0x4120	0	1	0	0						r/w	3/7	58
TemperatureExternal	1	0x4121	0	1	0	0						r/w	3/7	58
ResistorExternal	1/0	0x4122	0	1	0	0						r/w	3/7	58
OutputMode	1/0	0x4140	0	1	0	0						r/w	3/4	59
OutputPolarity	1/0	0x4141	0	1	0	0						r/w	3/4	59
VoltageMode	1	0x4142	0	1	0	0						r	3/7	60
CurrentMode	1	0x4143	0	1	0	0						r	3/7	60
VoltageModeList	1	0x4150	0	1	0	0						r	3/7	60
CurrentModeList	1	0x4160	0	1	0	0						r	3/7	61
GroupNumber	1/0	0x4200	0	1	0	0						w/r	3/4	61

Notes:
S DATA_ID type bit for a EDCP-frame of an access to a single channel
G DATA_ID type bit for a EDCP-frame of an access to a group of channels
M DATA_ID type bit for a EDCP-frame of an access to the whole module
1) Sn single channel access bits, (n=0..11)
2) x 0 or 1

LINKS PRÜFEN

6.4.2 EDCP Multiple Single Channels Access

Access	DATA_DIR	WORD	DATA_ID Bit									read / write / active	DATA-Bytes	Page
	ID0	hex	15	14	13	12	...	...	...	1	0			
DATA_ID			**0**	**S**	**G**	**M**	x [2]	x [2]	x [2]	x [2]	x [2]			
Single channel access	**1**	**0x6xxx**	**0**	**1**	**1**	**0**	**S11 ... S0** [1]							
ChannelStatus	1	0x6000	0	1	1	0	0					r	5/5	45
ChannelControl	1	0x6001	0	1	0	0	1					r	5/5	47
ChannelEventStatus	1	0x6002	0	1	1	0						r	5/5	48
ChannelEventMask	1	0x6003	0	1	1	0						r	5/5	50
DelayedTripAction	0/1	0x6006	0	1	1	0						w/r	3/4	51
DelayedTripTime	0/1	0x6005	0	1	1	0						w/r	3/5	52
ExternalInhibitAction	0/1	0x6007	0	1	1	0	0x007					w/r	3/4	53
VoltageSet	1	0x6100	0	1	1	0	0x100					r	5/7	54
CurrentSet / CurrentTrip	1	0x6101	0	1	1	0	0x101					r	5/7	54
VoltageMeasure	1	0x6102	0	1	1	0	0x102					r	5/7	55
CurrentMeasure	1	0x6103	0	1	1	0	0x103					r	5/7	55
VoltageBounds	1	0x6104	0	1	1	0	0x104					r	5/7	56
CurrentBounds	1	0x6105	0	1	1	0	0x105					r	5/7	56
VoltageNominal	1	0x6106	0	1	1	0	0x106					r	5/7	57
CurrentNominal	1	0x6107	0	1	1	0	0x107					r	5/7	57
CurrentMeasure Range	1	0x6109	0	1	1	0	0x109					r	3/8	57
VctCoefficient	1/0	0x6120	0	1	1	0	0X120					r/w	3/7	58
TemperatureExternal	1	0x6121	0	1	1	0	0X121					r/w	3/7	58
ResistorExternal	1/0	0x6122	0	1	1	0	0X122					r/w	3/7	58
OutputMode	1/0	0x6140	0	1	1	0	0X140					r/w	3/4	59
OutputPolarity	1/0	0x6141	0	1	1	0	0X141					r/w	3/4	59
VoltageMode	1	0x6142	0	1	1	0	0X142					r	3/7	60
CurrentMode	1	0x6143	0	1	1	0	0X143					r	3/7	60
VoltageModeList	1	0x6150	0	1	1	0	0X150					r	3/7	60
CurrentModeList	1	0x6160	0	1	1	0	0X150					r	3/7	61
ChannelGroup	0	0x6200	0	1	1	0	0X200					w	6	61

Notes:
S DATA_ID type bit for a EDCP-frame of an access to single channel
G DATA_ID type bit for a EDCP-frame of an access to a group of channels
M DATA_ID type bit for a EDCP-frame of an access to the whole module
[1] Sn single channel access bits, (n=0..11)
[2] x 0 or 1

LINKS prüfen.

6.4.3 Module Access

Access	DATA_DIR	WORD	DATA_ID Bit									read / write / active	DATA-Bytes	Page
	ID0	hex	15	14	13	12	...	...	...	1	0			
DATA_ID			**0**	**S**	**G**	**M**	x [2]	x [2]	x [2]	x [2]	x [2]			
Module access	**1/0**	**0x1xxx**	**0**	**0**	**0**	**1**	**M11 ... M0** [1]							
ModuleStatus	1	01000	0	0	0	1						r	2/4	62
ModuleControl		0x1001	0	0	0	1						w/r	4/2	63
ModuleControl32		0x1081	0	0	0	1							6/2	
ModuleEventStatus	1/0	0x1002	0	0	0	1						r/w	2/4	66
ModuleEventMask	0/1	0x1003	0	0	0	1						w/r	4/2	67
ModuleEventChannelStatus	1/0	0x1004	0	0	0	1						r/w	2/4	68
ModuleEventChannelMask	0/1	0x1005	0	0	0	1						w/r	4/2	69
ModuleEventGroupStatus	0/1	0x1006	0	0	0	1						r/w	2/4	70
ModuleEventGroupMask	0/1	0x1007	0	0	0	1						w/r	4/2	71
VoltageRampSpeed	0/1	0x1100	0	0	0	1						w/r	6/2	71
CurrentRampSpeed	0/1	0x1101	0	0	0	1						w/r	6/2	72
VoltageMax	r	0x1102	0	0	0	1						r	2/6	72
CurrentMax	r	0x1103	0	0	0	1						r	2/6	73
Supply24	r	0x1104	0	0	0	1						r	2/6	73
Supply5	r	0x1105	0	0	0	1						r	2/6	74
BoardTemperature	0/1	0x1106	0	0	0	1						r	2/6	74
ThresholdArmErrorDetect	0/1	0x1107	0	0	0	1						w/r	6/2	74
SerialNumber	1	0x1200	0	0	0	1						r	2/6	75
FirmwareRelease	1	0x1201	0	0	0	1						r	2/6	75
BitRate	0/1	0x1202	0	0	0	1						r	4/2	75
NameOfFirmware	1	0x1203	0	0	0	1						r	5/6	36
ADC SamplesPerSecond	0/1	0x1204	0	0	0	1						w/r	4/2	37
DigitalFilter	0/1	0x1205	0	0	0	1						w/r	4/2	37
ChannelNumber	1	0x1208	0	0	0	1						r	6	77
ArticleDescription	1	0x1209	0	0	0	1						r	8	78
ModuleOption	1	0x1280	0	0	0	1						r	6	78
ModuleOptionSpec	1	0x1290	0	0	0	1						r	7	79
ModuleCommMode												w	4	80
Factory settings												r/w	4/8	-

Notes:
S DATA_ID type bit for a EDCP-frame of an access to single channel
G DATA_ID type bit for a EDCP-frame of an access to a group of channels
M DATA_ID type bit for a EDCP-frame of an access to the whole module
[1] Mn module access bits, (n=0 .. 11)
[2] x 0 or 1

6.4.4 EDCP Group Accesses

Access	DATA_DIR	WORD	DATA_ID Bit									read / write / active	DATA-Bytes	Page
	ID0	hex	15	14	13	12	...	...	...	1	0			
DATA_ID			**0**	**S**	**G**	**M**	G11	...	...	Gn [1]	G0			
Groups SetGroup StatusGroup MonitorGroup TripGroup	0/1	0x2000	0	0	1	0						w/r	8/4	81
Temperatures	1	0x2001	0	0	1							r	7	90
SupplyMeasurements	1	0x2002	0	0	1							r	7	90
GroupVoltageLimits	1	0x2005	0	0	1							r	7	90
GroupCurrentLimits	1	0x2006	0	0	1							r	7	90
VoltageSetAllChannels	0	0x2100	0	0	1							w	6	91
CurrentSetAllChannels	0	0x2101	0	0	1							w	6	91
SetOnOffAllChs		0x2200	0	0	1							r/w	6	92
SetEmergencyAllChs		0x2201	0	0	1							r/w	6	93
EventStatusVLimtAllChs		0x2202	0	0	1							r/w	6	94
EventStatusCLimtAllChs		0x2203	0	0	1							r/w	6	95
EventStatusTrpAllChs		0x2204	0	0	1							r/w	6	96
EventStatusInhAllChs		0x2205	0	0	1							r/w	6	97
SetOnOffChsExtender		0x2280	0	0	1							r/w	6	98
SetEmergencyChsExten.		0x2290	0	0	1							r/w	6	99

Notes:
S DATA_ID type bit for a EDCP-frame of an access to a single channel
G DATA_ID type bit for a EDCP-frame of an access to a group of channels
M DATA_ID type bit for a EDCP-frame of an access to the whole module
[1] Gn group access bits,(n=0 .. 11)

6.4.5 Important DCP Module Access

Access	EXT_ INSTR	DATA_ DIR	Byte	DATA_ID Bit								read / write / active	DATA-Bytes	Page
	ID0	ID1		7	6	5	4	3	2	1	0			
Group access MODULE:	0	1/0		1	1	M3	M2	M1	M0	R1	R0			
GeneralStatus	0	1/0	0xc0	1	1	0	0	0	0	0	0	a	3	100
LogOnOff Front-end at the superior layer	0	1/0	0xD8	1	1	0	1	1	0	0	0	a/w	3	102
Notes:														

6.5 Description of data information per DATA_ID in EDCP

6.5.1 EDCP Single Access

The single access describes the control of the channel properties. The range of the single access contains the accesses to the analog digital data items, to the status and the control words of the channels.

6.5.1.1 Channel status (single/multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master single read-	1	0x4000	Mx		
master single MBR read-	1	0x6000	Member		Offset
HV board write access	0	0x4000/0x6000	Mx	ChannelStatus	

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... too access up to 255 channels
ChannelStatus	DATA_0 to DATA_1	UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
isVLIM	isCLIM	isTRP	isEINH	isVBND	isCBND	isArcErr	isLCR
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
isCV	isCC	isEMCY	isRAMP	isON	IERR	isArc	Reserved

The ChannelStatus register describes the actual status. Depending on the status of the module the bits will be set or reset.
The bit InputError will be set if the given parameter is not plausible or it exceeds the module parameters (e.g. if the command Vset=4000V is given to a module with NominalVoltage=3000V). The bit InputError is not be set if the given values are temporarily not possible (e.g. Vset=2800 at a module with NominalVoltage=3000V, but HardwareLimitVoltage=2500V). A certain signature which kind of input error it is does not exists.

Bit	Name	Description
isVLIM	IsVoltageLimitExceeded	voltage limit set by Vmax is exceeded isVLIM=0 channel is ok isVLIM=1 the hardware voltage limit is exceeded
IsCLIM	IsCurrentLimitExceeded	current limit set by Imax is exceeded isCLIM=0 channel is ok isCLIM=1 the hardware current limit is exceeded (to detect a hardware voltage or current limit error flag the firmware has to evaluate the channel voltage and current at first)
isTRP	IsTripExceeded	Trip is set when Voltage or Current limit or Iset has been exceeded (when KillEnable=1) isTRP=0 channel is ok isTRP=1 VO is shut off to 0V without ramp because the channel has been tripped.

Bit	Name	Description
isEINH	IsExternalInhibit	External Inhibit isEINH=0 channel is ok isEINH=1 External Inhibit was scanned
isVBND	IsVoltageBoundsExceeded	Voltage out of bounds isVBND=0 channel is ok isVBND=1 $\lvert V_{meas}-V_{set}\rvert > V_{bounds}$
isCBND	IsCurrentBoundsExceeded	Current out of bounds IsCBND=0 channel is ok isCBND=1 $\lvert I_{meas} - I_{set}\rvert > I_{bounds}$ (to detect a voltage or current out of bound flag the firmware has to ramp the channel voltage V_{set} at first)
isArcErr	IsArcError	maximum number of allowed arcs is exceeded, high voltage has been turned off isArcErr=0 no arc error isArcErr=1 maximum number of allowed arcs is exceeded
isLCR	IsLowCurrentRange	Low or small current range of the current measurement isLCR=0 high or standard current range isLCR=1 low current range of the current measurement
isCV	IsControlledVoltage	Voltage control active (evaluation is guaranteed when no ramp is running) sCV=1 channel is in state of voltage control isCC=1 channel is in state of current control
isCC	IsControlledCurrent	Current control active (evaluation is guaranteed when no ramp is running)
isEMCY	IsEmergencyOff	Emergency off without ramp isEMCY=1 channel is in state of emergency off, VO has been shut off to 0V without ramp
isON	IsOn	On isON=0 channel is off isON=1 channel voltage follows the Vset value
isRAMP	IsRamping	Ramp is running isRAMP=0 no voltage is in change isRAMP=1 voltage is in change with the stored ramp speed value
IERR	InputError	Input error IERR=0 no input-error IERR=1 incorrect message to control the channel
IsArc	isArc or IsRegulationError	at least one electrical arc is active or faster error detection of the channel hardware is not in regulation (updated by firmware every 5ms) isARC=0 no arc active / normal error evaluation isARC=1 at least one electrical arc is active / fast detection of a regulation error (OPTION)
res	reserved	

6.5.1.2 Channel control: (single write- and single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master write access	0	0x4001	Mx		
master read-	1	0x4001	Mx	ChannelControl	
master single MBR read-	1	0x6001	Member		Offset
HV board write access	0	0x4001/0x6001	Mx	ChannelControl	

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels

ChannelControl DATA_0 to DATA_1 UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
Reserved	Reserved	setEMCY	Reserved	setON	Reserved	Reserved	Reserved

The signals SetOn and SetEmergencyOff control are basic functions of the channel. The signal SetOn is switching ON the HV of the channel and is a precondition for giving voltage to the output. As far as a VoltageSet has been set and no event has occurred and is not registered yet (in minimum, bit 5 and bit 10 to 15 of the register Channel Event Status must be 0), a start of a HV ramp will be synchronized (a ramp is a software controlled, time proportionally increase / decrease of the output voltage).
A SetEmergencyOff switch the channel in state isEmergencyOff and a new SetOn is only possible after SetEmergencyOff is reset to zero.

Bit	Name	Description
setEMCY	SetEmergencyOff	Set “Emergency Off” SetEMCY=0 channel emergency cut-off works setEMCY=1 cut-off VO shut off to 0V without ramp
setON	SetOn	Set On
		setOn=0 switch the channel to OFF setOn=1 switch the channel to ON
res	Reserved	

6.5.1.3 Channel event status (single write- and single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master write access	0	0x4002	Mx		
master read-	1	0x4002	Mx	ChannelEventStatus	
master single MBR read-	1	0x6002	Member		Offset
HV board write access	0	0x4002/0x6002	Mx	ChannelEventStatus	

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels

ChannelEventStatus DATA_0 to DATA_1 UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
EVLIM	ECLIM	ETRP	EEINH	EVBNDs	ECBNDs	EAE	Reserved
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
ECV	ECC	EEMCY	EEOR	EOn2Off	EIER	EARC	Reserved

Bit	Name	Description
EVLIM	EventVoltageLimit	Event: Hardware- voltage limit has been exceeded
ECLIM	EventCurrentLimit	Event: Hardware- current limit has been exceeded
ECLIM	EventCurrentLimit	Event: Hardware- current limit has been exceeded
ETRP	EventTrip	Event: Trip is set when Voltage or Current limit or Iset has been exceeded (when KillEnable=1 or Delayed Trip is configured)
EEINH	EventExternalInhibit	Event external Inhibit
EVBNDs	EventVoltageBounds	Event: Voltage out of bounds
ECBNDs	EventCurrentBounds	Event: Current out of bounds
EAE	EventArcError	Event: Arc Error
ECV	EventControlledVoltage	Event: Voltage control
ECC	EventControlledCurrent	Event: Current control
EEMCY	EventEmergencyOff	Event: Emergency off
EEOR	EventEndOfRamp	Event: End of ramp
EOn2Off	EventOnToOff	Event: Change from state "On" to "Off" without ramp
EIER	EventInputError	Event: Input Error
EARC	EventArc	Event: Arc active or Regulation Error (Option - fast error evaluation)

An event bit is permanently set if the status bit is 1 or is changing to 1. Different to the status bit an event bit isn't automatically reset. A reset has to be done by the user by writing an 1 to this event bit.

6.5.1.4 Channel event mask (single write- and single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master write access	0	0x4003	Mx		
master read-	1	0x4003	Mx	ChannelEventMask	
master single MBR read-	1	0x6003	Member		Offset
HV board write access	0	0x4003/0x6003	Mx	ChannelEventMask	

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels
ChannelEventMask	DATA_0 to DATA_1	UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
MEVLIM	MECLIM	MECTRP	MEEINH	MEVBNDs	MECBNDs	MEARC	Reserved
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
MECV	MECC	Reserved	MEEOR	MEOn2Off	MEIERR	MEARC	Reserved

The function of the ChannelEventMask register is described in 6.5.5.1Channel events

Bit	Name	Description
MEVLIM	MaskEventVoltageLimit	EventMask: Hardware- voltage limit has been exceeded
MECLIM	MaskEventCurrentLimit	EventMask: Hardware- current limit has been exceeded
METRIP	MaskEventTrip	EventMask: Voltage limit or Current limit or Iset has been exceeded (when KillEnable=1)
MEEINH	MaskEventExtInhibit	EventMask: External Inhibit
MEVBNDs	MaskEventVoltageBounds	EventMask: Voltage out of bounds
MECBNDs	MaskEventCurrentBounds	EventMask: Current out of bounds
MEARC	MaskEventArcError	EventMask: Arc error
MECV	MaskEventControlledVoltage	EventMask: Voltage control
MECC	MaskEventControlledCurrent	EventMask: Current control
MEEMCY	MaskEventEmergencyOff	EventMask: Emergency off
MEEOR	MaskEventEndOfRamp	EventMask: End of ramp
MEOn2Off	MaskEventOnToOff	EventMask: Change from state on to off without ramp
MEIER	MaskEventInputError	EventMask: Input Error
MARC	MaskEventArc MaskEventRegulationError	EventMask: Arc active EventMask: Regulation Error (Option - fast error evaluation)

CAUTION!
 CAUTION! Module in mode KILL disable: If a bit of the ChannelEventStatus register is set to “1” and the corresponding bit in the ChannelEventMask register is “0”, it is not necessary to clear the ChannelEventStatus bit to switch on HV again.

If a bit of the ChannelEventMask register is set to “1” and if the corresponding bit in the ChannelEventStatus is set to “1” by the module firmware then a reset of the corresponding ChannelEventStatus bits is necessary before a switch on the HV of this channel is possible again.

Module in mode KILL enable: A reset of the ChannelEventStatus bits is necessary before switch on the HV of this channel again.

6.5.1.5 Delayed trip action (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_0	DATA_1	DATA_2
master write access	0	0x4006	Mx	Action		
master read-	1	0x4006	Mx			
master single MBR read-	1	0x6006	Member		Offset	Action
HV board write access	0	0x4006	Mx	Action		

Notes:

Mx	Channel	0 … 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … to access up to 255 channels

Action	Action if a trip event will be initiated
0	no action
1	ramp down high voltage of the channel
2	shut down high voltage of the channel without ramp
3	shut down the whole module without ramp
4	switch off the delayed trip function

6.5.1.6 Delayed trip time

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_1	DATA_0
master single read-	1	0x4005	Mx		
master single MBR read-	1	0x4005	Member		Offset
HV board write access	0	0x4005 / 0x6003	Mx		

Notes:

Mx	Channel	0 … 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … to access up to 255 channels

Timeout-time DATA_0 to DATA_1[ms] UI2 (Range 1 to 4095 ms)

Time in milliseconds until delayed trip action becomes active and channel is in current control state. Note special functionality for modules with a second low current range – see manual “Delayed trip EHS.pdf”.

6.5.1.7 External channel inhibit

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_0	DATA_1	DATA_2
master write access	0	0x4007	Mx	Action		
master read-	1	0x4007	Mx			
master single MBR write-	1	0x6007	Member		Offset	Action
HV board write access	0	0x4007 / 0x6007	Mx	Action		

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels

Action	Action if an inhibit signal will be triggered
0	no action
1	ramp down high voltage of the channel
2	shut down high voltage of the channel without ramp
3	shut down the whole module without ramp
4	switch off the external inhibit function

6.5.1.8 Set voltage (single write- and single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4100	Mx	VoltageSet			
master read -	1	0x4100	Mx				
master single MBR read-	1	0x6100	Member		Offset		
HV board write access	0	0x4100/0x6100	Mx	VoltageSet			

Notes:

Mx	Channel	0 … 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … to access up to 255 channels
VoltageSet	DATA_0 to DATA_3 [V]	R4

The VoltageSet value is the preset for voltage generation. Allowed values are between 0 and the actual hardware limit value. If written values are between the hardware limit and the nominal value, then the module reduces these values to the value of the actual hardware limit. If written values are higher than the nominal data or lower than 0 an input error is indicated by setting the bit InputError.

If the channel is switched 'ON' then the voltage will be ramped to the set value after the receipt of this access. Otherwise the set value will just be stored and only used for ramping to the set voltage after the channel will be switched 'ON'.

6.5.1.9 Set current / trip (single write- and single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4101	Mx	CurrentSet (CurrentTrip)			
master read -	1	0x4101	Mx				
master single MBR read-	1	0x6101	Member		Offset		
HV board write access	0	0x4101/0x6101	Mx	CurrentSet (CurrentTrip)			

Notes:

Mx	Channel	0 … 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … to access up to 255 channels
CurrentSet (CurrentTrip)	DATA_0 to DATA_3 [A]	R4

Allowed values are between 0 and the actual hardware limit value. If written values are between the hardware limit and the nominal value, then the module reduces these values to the value of the actual hardware limit. If written values are higher than the nominal data or lower than 0 an input error is indicated by setting the bit InputError.

The mode of action of this item depends on the setting of the signal Kill Enable (KILEna) in the ModuleControl register (6.5.2.2). If Kill Enable is 0, the value is interpreted as CurrentSet. If Kill Enable is 1, the value is CurrentTrip.

CurrentSet:

The CurrentSet value is the preset for current regulation. If the output current reaches or exceeds the Current Set value, the channel goes into Current Regulation mode. In this mode the output current is regulated at the CurrentSet value, but the output voltage is going to a value between 0V and Vset, depending of the external load.

When Current Control mode is active the bit isCC of the ChannelStatus register and the bit EventControlledCurrent of the ChannelEventStatus are set, the bit isCV of the ChannelStatus is reset.

CurrentTrip:

In Current Trip mode this value will be used as software current trip. If exceeding this value a current trip event will be registered. The green LED on front panel will be switched off.

The bits isTrip in the ChannelStatus and ETRP in ChannelEventStatus are set, the bit isNoSumError in the ModuleStatus is reset.

6.5.1.10 Voltage measurement (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4102	Mx				
master single MBR read-	1	0x6102	Member		Offset		
HV board write access	0	0x4102/0x6102	Mx	VoltageMeasure			

Notes:

Mx	Channel	0 … 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … to access up to 255 channels
VoltageMeasure	DATA_0 to DATA_3 [V]	R4

6.5.1.11 Current measurement (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4103	Mx				
master single MBR read-	1	0x6103	Member		Offset		
HV board write access	0	0x4103/0x6103	Mx	CurrentMeasure			

Notes:

Mx	Channel	0 … 255
Member	Members	1 … 16
Offset	Channel member offset	0, 16, 32 … to access up to 255 channels
CurrentMeasure	DATA_0 to DATA_3 [A]	R4

6.5.1.12 Voltage bounds (single write- / single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4104	MX	VoltageBounds			
master read -	1	0x4104	MX				
master single MBR read-	1	0x6104	Member		Offset		
HV board write access	0	0x4104 / 0x6104	MX	VoltageBounds			

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels
VoltageBounds	DATA_0 to DATA_3 [V]	R4 (0 to VoltageNominal)

6.5.1.13 Current bounds (single write- / single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4105	MX	CurrentBounds			
master read -	1	0x4105	MX				
master single MBR read-	1	0x6105	Member		Offset		
HV board write access	0	0x4105 / 0x6105	MX	CurrentBounds			

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels
CurrentBounds	DATA_0 to DATA_3 [A]	R4 (0 to CurrentNominal)

6.5.1.14 Nominal voltage (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4106	MX				
master single MBR read-	1	0x6106	Member		Offset		
HV board write access	0	0x4106 / 0x6106	MX	VoltageNominal			

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels
VoltageNominal	DATA_0 to DATA_3 [V]	R4

6.5.1.15 Nominal current (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4107	MX				
master single MBR read-	1	0x6107	Member		Offset		
HV board write access	0	0x4107 / 0x6107	MX	CurrentNominal			

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels
CurrentNominal	DATA_0 to DATA_3 [A]	R4

6.5.1.16 Current measurement range[1] (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_4	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4109	MX					
master single MBR read-	1	0x6109	Member		Offset			
HV board write access	0	0x4109 / 0x6109	MX	CurrentMeasure				Range

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels
CurrentMeasure	DATA_1 to DATA_4 [A]	R4
Range	DATA_0=0 – high range (≥20µA) DATA_0=1 – low range (<20µA)	UI1

INFORMATION

INOTE

The information channel status bit isLowCurrentRange can be used also.

1 for device class 26, 27 and 39, E08F2, E08C2 and N06C2 only

6.5.1.17 VCT Coefficient[2] (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4120	Mx	VctCoefficient			
master read -	1	0x4120	Mx				
master single MBR read-	1	0x6120	Member		Offset		
HV board write access	0	0x4120/0x6120	Mx	VctCoefficient			

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels
VctCoefficient	DATA_0 to DATA_3 [V/K]	R4

6.5.1.18 Temperature external[3] (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4121	Mx				
master single MBR read-	1	0x6121	Member		Offset		
HV board write access	0	0x4121/0x6121	Mx	TemperatureExternal			

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels
TemperatureExternal	DATA_0 to DATA_3 [°C]	R4

2 Option VCT only
3 Option VCT only

6.5.1.19 Resistor external[4] (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x4122	MX	ResistorExternal			
master read -	1	0x4122	Mx				
master single MBR read-	1	0x6122	Member		Offset		
HV board write access	0	0x4122/0x6122	Mx	ResistorExternal			

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels
ResistorExternal	DATA_0 to DATA_3 [Ω]	R4

6.5.1.20 Output mode[5] (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_0
master write access	0	0x4140	Mx	Mode
master read -	1	0x4140	Mx	
master single MBR read-	1	0x6140	Member	Offset
HV board write access	0	0x4120/0x6120	Mx	Mode

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels
Mode	DATA_0 UI1	(HV MODE = 1, 2 or 3)

6.5.1.21 Output polarity[6] (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_0
master write access	0	0x4141	Mx	Polarity
master read -	1	0x4141	Mx	
master single MBR read-	1	0x6141	Member	Offset
HV board write access	0	0x4121/0x6121	Mx	Polarity

Notes:

Mx	Channel	0 ... 255
Member	Members	1 ... 16
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels
Polarity	DATA_0 SI1	(Positive = +1, Negative = -1)

4 Option EHS STACK
5 Option HV-MODE SWITCHABLE
6 Option POLARITY SWITCHABLE

6.5.1.22 Output voltage mode[7] (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4142	Mx				
master single MBR read-	1	0x6142	Member		Offset		
HV board write access	0	0x4142/0x6142	Mx	VoltageMode			

Notes:

Mx	Channel	0 ... 255	
Member	Members	1 ... 16	
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels	
VoltageMode	DATA_0 to DATA_3 [V]	R4	(+6000, +4000, +2000, -2000, -4000 or -6000)

6.5.1.23 Output current mode[8] (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4143	Mx				
master single MBR read-	1	0x6143	Member		Offset		
HV board write access	0	0x4143/0x6143	Mx	CurrentMode			

Notes:

Mx	Channel	0 ... 255	
Member	Members	1 ... 16	
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels	
VoltageMode	DATA_0 to DATA_3 [A]	R4	(+4.0E-3, +3.0E-3, +2.0E-3, +0.1E-3, -0.1E-3,-2.0E-3, -3.0E-3 or -4.0E-3)

6.5.1.24 Output voltage mode list[9] (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4150 - 0x415f	Mx				
master single MBR read-	1	0x6150 - 0x415f	Member		Offset		
HV board write access	0	0x4150/0x6150	Mx	VoltageModeList			

Notes:

Mx	Channel	0 ... 255	
Member	Members	1 ... 16	
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels	
VoltageModeList	DATA_0 to DATA_3 [V]	R4	(+6000, +4000, +2000, -2000, -4000 or -6000)

7 Option HV-MODE SWITCHABLE
8 Option HV-MODE SWITCHABLE
9 Option HV-MODE SWITCHABLE

6.5.1.25 Output current mode list[10] (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x4143	Mx				
master single MBR read-	1	0x6143	Member		Offset		
HV board write access	0	0x4143/0x6143	Mx	CurrentMode			

Notes:

Mx	Channel	0 ... 255	
Member	Members	1 ... 16	
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels	
VoltageMode	DATA_0 to DATA_3 [A]	R4	(+4.0E-3, +3.0E-3, +2.0E-3, +0.1E-3, -0.1E-3,-2.0E-3, -3.0E-3 or -4.0E-3)

6.5.1.26 Group number (single/ multiple single read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	CHN	DATA_0		
master write access	0	0x4200	Mx	GROUP		
master read -	1	0x4200	Mx			
master single MBR read-	1	0x6200	Member		Offset	GROUP
HV board write access	0	0x4200	Mx	GROUP		

Notes:

Mx	Channel	0 ... 255	
Member	Members	1 ... 16	
Offset	Channel member offset	0, 16, 32 ... to access up to 255 channels	
Group	Group number of the channel members	0 .. 255	

With a group number GROUP for each channel, channels can be combined to groups involving all connected modules. The NMT channel group set and the NMT module set frames (described on page 19) send broadcast information for all channels, which have the same group number.

10 Option HV-MODE SWITCHABLE

6.5.2 EDCP Module Accesses

6.5.2.1 ModuleStatus (module read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_1	DATA_1
master read-	1	0x1000		
HV board write access	0	0x1000	ModuleStatus	
Notes: ModuleStatus DATA_0 to DATA_1 UI2				

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
isKillE	isTmpGd	isSplyGd	isModGd	isEvntAct	isSflpGd	isNoRamp	isNoSumErr
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
Reserved	isInErr	isHwVlGd	needSrvc	isHvOn	isLvIns	res	isAdj

The status bits as there are IsTemperatureGood, IsSupplyGood, IsModuleGood, IsEventActive, IsSafetyLoopGood, IsNoRamp and IsNoSumError indicate the single status for the complete module.

The status bit IsCommandComplete indicates whether all CAN commands given to the module have been executed.

Bit	Name	Description
isKillE	IsKillEnable	Module state of kill enable isKillEna=0 Module in state kill disable isKillEna=1 Module in state kill enable
isTmpGd	IsTemperatureGood	Module temperature good isTmpGd=0 If module temperature is higher than 55°C then all channel are switched off permanently isTmpGd=1 module temperature is within working range
isSplyGd	IsSupplyGood	Power supply good IsSplyGd=0 supply voltages are out of range (range of24V +/-10% and of 5V +/-5%) isSplyGd=1 supply voltages are within range

Bit	Name	Description
isModGd	IsModuleGood	Module in state good isModGd=0 module is not good, that means (isnoSERR AND (ETMPngd OR ESPLYngd OR ESFLPngd))==0 isModGd=1 module is good, that means (isnoSERR AND NOT(ETMPngd OR ESPLYngd OR ESFLPngd))==1(see module event status also)

Bit	Name	Description
isEvntAct	IsEventActive	Any event is active and mask is set isEvntAct=0 no Event is active isEvntAct=1 any Event is active
isSflpGd	IsSafetyLoopGood	Safety loop closed isSflpGd=0 safety loop is broken -VO bas been shut off, isSflpGd=1 safety loop is closed
isNoRamp	IsNoRamp	All channels stable, no ramp active isNoRamp=0 VO is ramping in at least one channel isNoRamp=1 no channel is ramping
isNoSumErr	IsNoSumError	All channels without failure isNoSumErr=0 voltage limit, current limit, trip, voltage bound or current bound has been exceeded in at least one of the channels or external INHIBIT ➜ error, reset by reset of the corresponding flag of the channel status' isnoSumERR=1 evaluation of the 'Channel Status' over all channels to a sum error flag ➜ LIM&CLIM&CTRP&EINH&VBND&CBND=0 ➜ no errors
isInErr	IsInputError	Input error in connection with a module access isInErr=1 input error in connection with a module access isInErr=0 no input error in connection with a module access
isHwVlGd	IsHardwareVoltageLimitGood	Hardware voltage limit in proper range, forHV distributor modules with current mirror only isHwVlGd=0 hardware voltage limit not in proper range isHwVlGd=1 hardware voltage limit in proper range
needSrvc	IsServiceNeeded	Hardware failure detected (consult iseg Spezialelektronik GmbH) needSrvc=0 Module is ready for working needSrvc=1 Module need a service
isHvOn	IsHighVoltageOn	At least one channel generates a high voltage isHvOn=0 No high voltage will be generated isHvOn=1 At least one channel generates a high voltage output. Modules with 7 digit serial number only.
isLvIns	IsLiveInsertion	Mode live insertion isLvIns=0 no Live Insertion mode isLvIns=1 Live Insertion mode
isAdj	IsFineAdjustment	Mode of the fine adjustment
		isAdj=0 Fine adjustment is off. isAdj=0 Fine adjustment is on (default).
res	Reserved	

6.5.2.2 ModuleControl (module write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write access	0	0x1001	ModuleControl	

master read-	1	0x1001	
HV board write access	0	0x1001	ModuleControl
Notes: ModuleControl DATA_0 to DATA_1 (Bit 0 -15) UI2			

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write	0	0x1081	ModuleControl32			
master read-	1	0x1081				
HV board write access	0	0x1081	ModuleControl32			
Notes: ModuleControl32 DATA_0 to DATA_3 (Bit 0 -31) UI4						

Diese Tabelle ist NEU. Nicht im 2017 Dokument.

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	setR3	disVL
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
Reserved	setKILena	setR2	setADJ	set ENDN	Reserved	Reserved	Reserved
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
setR1	doCLEAR	setILK	doMux	Reserved	Reserved	Reserved	Reserved

Bit	Name	Description
setR3	SetRelayThree	
disVL	DisableVoltageRampSpeedLimit	Switch off voltage ramp speed limitation
setKILena	KillEnable	Kill function SetKILL = 0 kill function disable setKILL = 1 kill function enable
setADJ	Adjust	Switch ON of fine adjustment setADJ = 0 fine adjustment OFF setADJ = 1 fine adjustment ON
setENDN	Endian	Order of bytes in word: 0 = Little Endian (INTEL); 1 = Big Endian (MOTOROLA) setENDN = 1 big endian (MOTOROLA format)
doCLEAR	ClearKill	Hardware ClearKill signal and clear all event signals of module and channels doCLEAR =1 Hardware ClearKill signal and clear all event signals of the module and the channels doCLEAR=0 no action
setILK	Interlock	Interlock signal CRATE_ENABLE (WIENER MPOD crate, active TTL high) setILK= 1 INTERLOCK signal in order to switch off HV and set bit EEINH of the EventStatus for all channels setILK=0 reset the INTERLOCK signal in order to clear the bit EEINH of the EventStatus for all channels
doMux	DoMultiplex	Switch on multiplexing, for electronic load (EZL) only

Bit	Name	Description
		doMux = 0 switch off multiplexing doMux = 1 switch on multiplexing
setR1	SetRelayOne	Switch on load one, for electronic load (EZL) only
setR2	SetRelayTwo	Switch on load two, for electronic load (EZL) only
		setR1/2/3 = 0 switch off load 1, 2 or 3 setR1/2/3 = 1 switch on load 1, 2 or 3
res	Reserved	

6.5.2.3 ModuleEventStatus (module write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1002	ModuleEventStatus	
master read-	1	0x1002		
HV board write access	0	0x1002	ModuleEventStatus	
Notes: ModuleEventStatus	DATA_0 to DATA_1	UI2		

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
Reserved	ETMPngd	ESPLYngd	Reserved	Reserved	ESFLPngd	Reserved	Reserved
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
Reserved	EIERR	EHwVLngd	ESrvc	Reserved	ELVINS	Reserved	Reserved

Bit	Name	Description
ETMPngd	EventTemperatureNotGood	Event: Temperature is above 55°C
ESPLYngd	EventSupplyNotGood	Event: at least one of the supplies is not good
ESFLPngd	EventSafetyLoopNotGood	Event: Safety loop is open
EIERR	EventInputError	Event: input error in connection with a module access
EHwVLngd	EventHardwareVoltageLimitNotGood	Event: Hardware voltage limit is not in proper range, only for HV distributor modules with current mirror;
ESrvs	EventService	Event: A hardware failure of the HV module has been detected. The HV will switched off without a possibility to switch on again. Please consult the iseg Spzialelektronik GmbH.
ELVINS	EventLiveInsertion	Event live insertion to prepare a hot plug of a module
res	Reserved	

6.5.2.4 ModuleEventMask (module write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1003	ModuleEventMask	
master read-	1	0x1003		
HV board write access	0	0x1003	ModuleEventMask	
Notes: ModuleEventMask	DATA_0 to DATA_1	UI2		

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
Reserved	METMPngd	MESPLYngd	Reserved	Reserved	MESFLPngd	Reserved	Reserved
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
Reserved	MEIERR	MEHwVLngd	Reserved	Reserved	Reserved	Reserved	Reserved

Bit	Name	Description
METMPngd	MaskEventTemperatureNotGood	MEventMask: Temperature is above 55°C
MESPLYngd	MaskEventSupplyNotGood	MEventMask: at least one of the supplies is not good
MESFLPngd	MaskEventSafetyLoopNotGood	MEventMask: Safety loop (SL) is open
MEIERR	MaskEventInputError	MEventMask: Input error in connection with a module access
MEHwVLngd	MaskEventHardwareVoltageLimitNotGood	MEventMask: Hardware voltage limit is not in proper range, only for HV distributor modules with current mirror;
res	Reserved	

All bits of the EventMask register are set to “0” after the power on reset.

Module in mode KILL enable: If a bit of the EventStatus register is set to “1” and the corresponding bit in the EventMask register is “0” no reset of the EventStatus bits is necessary before switch on the HV of any channel again.

If a bit of the EventMask register is set to “1” and if the corresponding bit in the EventStatus is set to “1” by the module firmware a reset of the corresponding EventStatus bits is necessary before a switch on the HV of any channel is possible.

Module in mode KILL enable: A reset of the EventStatus bits is necessary before switch on the HV of any channel is possible.

6.5.2.5 ModuleEventChannelStatus (module write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_2	DATA_1	DATA_0
master write access	0	0x1004	Offset	ModuleEventChannelStatus	
master read-	1	0x1004	Offset		
HV board write access	0	0x1004	Offset	ModuleEventChannelStatus	
Notes: Offset EventChannelStatus	DATA_2Channel member offset DATA_0 to DATA_1 UI2		0, 16, 32 ... access up to 255 channels		

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH15	CH14	Ch13	CH12	CH11	CH10	CH9	CH8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

The n-th bit of the register is set, if an event is active in the n-th channel and the associated bit in the EventMask register of the n-th channel is set too.

CHn = EventStatus[n] & EventMask[n]

Reset of a bit is done by writing a 1 to this bit.

6.5.2.6 ModuleEventChannelMask (module write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_2	DATA_1	DATA_0
master write access	0	0x1005	Offset	ModuleEventChannelMask	
master read-	1	0x1005	Offset		
HV board write access	0	0x1005	Offset	ModuleEventChannelMask	
Notes: Offset EventChannelMask		DATA_2Channel member offset DATA_0 to DATA_1		0, 16, 32 ... access up to 255 channels UI2	

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH15	CH14	Ch13	CH12	CH11	CH10	CH9	CH8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

This register decides whether a pending event leads to the sum event flag of the module or not. If the n-th bit of the mask is set and the n-th channel has an active event in the ModuleEventChannelStatus the bit isEventActive in the ModuleStatus register is set.

6.5.2.7 ModuleEventGroupStatus (module write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1005	ModuleEventGroupStatus			
master read-	1	0x1005				
HV board write access	0	0x1005	ModuleEventGroupStatus			
Notes: EventGroupStatus	DATA_0 to DATA_3	UI4				

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
GR31	GR30	GR29	GR28	GR27	GR26	GR25	GR24
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
GR23	GR22	GR21	GR20	GR19	GR18	GR17	GR16
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
GR15	GR14	GR13	GR12	GR11	GR10	GR9	GR8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
GR7	GR6	GR5	GR4	GR3	GR2	GR1	GR0

The n-th bit of this double word register is set, if an event is active in the n-th group.

Reset of a bit is done by writing a 1 to this bit.

6.5.2.8 ModuleEventGroupMask (module write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1006	ModuleEventGroupMask			
master read-	1	0x1006				
HV board write access	0	0x1006	ModuleEventGroupMask			
Notes: EventGroupMask	DATA_0 to DATA_3	UI4				

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
GR31	GR30	GR29	GR28	GR27	GR26	GR25	GR24
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
GR23	GR22	GR21	GR20	GR19	GR18	GR17	GR16
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
GR15	GR14	GR13	GR12	GR11	GR10	GR9	GR8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
GR7	GR6	GR5	GR4	GR3	GR2	GR1	GR0

This register decides whether a pending event leads to the sum event flag of the module or not. If the n-th bit of the mask is set and the n-th group has an active event in the ModuleEventGroupStatus the bit isEventActive in the ModuleStatus register is set.

6.5.2.9 VoltageRampSpeed (module write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1100	VoltageRampSpeed			
master read-	1	0x1100				
HV board write access	0	0x1100	VoltageRampSpeed			
Notes: VoltageRampSpeed	DATA_0 to DATA_3 [%]	R4				

Voltage ramp speed range (disable Kill)	1mV/s ≤ Ramp speed ≤ 20% of VO max/s	
Option: fast ramp	1	1mV/s ≤ Ramp speed ≤ 25% of VoltageNominal
	2	1mV/s ≤ Ramp speed ≤ 50% of VoltageNominal
	3	1mV/s ≤ Ramp speed ≤ 75% of VoltageNominal

Voltage ramp speed range (enable Kill): 1mV/s ≤ Ramp speed ≤ 1% of $V_{O\,max}$/s
The speed of the voltage ramp in percent of the nominal voltage of the channel per second.

6.5.2.10 CurrentRampSpeed – current controlled modules only (module write- / read-write access)

EDCP frame

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1101	CurrentRampSpeed			
master read-	1	0x1101				
HV board write access	0	0x1101	CurrentRampSpeed			
Notes: CurrentRampSpeed	DATA_0 to DATA_3 [%]	R4				

Current ramp speed range: 2 % IO max/s ≤ Ramp speed ≤ IO max/s

The speed of the current ramp in percent of the nominal current of the channel per second.

6.5.2.11 VoltageMax – OPTION (module read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read-	1	0x1102				
HV board write access	0	0x1102	VoltageMax			
Notes: HardwareVoltageLimit	DATA_0 to DATA_3 [%]	R4				

HV Modules with the OPTION hardware voltage limit can adjust VO max via the potentiometer Vmax.

For HV Modules without this OPTION VoltageMax equals to VO max.

The exceeding of the hardware voltage limit results in a limitation of the voltage when the KILL-enable.

The absolute value of the hardware voltage limit will compute by following:

Voltage limit of the channel x (Chx) = VoltageNominal[Chx] • VoltageMax

The module responds after the hardware voltage limit has been exceeded:

The green LED on front panel is off.

Depends of the kind of module:

Hardware KILL function controlled by the bit 'KILena' of the ModuleControl word:

KILL-enable = 1:	The voltage will be switched off permanently without ramp. ChannelEventStatus flag 'EVLIM' will be set.
KILL-enable = 0:	The voltage will be reduced to the value of the actual hardware voltage limit. ChannelStatus flag 'isVLIM' and ChannelEventStatus flag 'EVLIM' will be set.

Software KILL function controlled by the bit 'KILena' of the ChannelControl word:

KILL-enable = 1:	Voltage will be switched off permanently without ramp. ChannelEventStatus flag 'EVLIM' will be set.
KILL-enable = 0:	Voltage will be switched off without ramp. If the output voltage arrives at 0 V the ramping to set voltage will be restarted automatically. ChannelStatus flag 'isVLIM' and ChannelEventStatus flag 'EVLIM' will be set.

6.5.2.12 CurrentMax – OPTION (module read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read-	1	0x1103				
HV board write access	0	0x1103	CurrentMax			
Notes: HardwareCurrentLimit DATA_0 to DATA_3 [%] R4						

HV Modules with the OPTION CurrentMax can adjust the IO max via the potentiometer Imax.

HV Modules without this OPTION deliver IO max.

The absolute value of the hardware current limit will compute by following:

Current limit of the channel x (Chx) = CurrentNominal[Chx] • CurrentMax

The module responds after the hardware current limit has been exceeded:

The green LED on front panel is off.

Depends of the kind of module:

Hardware KILL function controlled by the bit 'KILena' of the ModuleControl word:

KILL-enable = 1:	Voltage will be switched off permanently without ramp. ChannelEventStatus flag 'ECLIM' will be set.
KILL-enable = 0:	Current will be reduced to the value of the actual hardware current limit. ChannelStatus flag 'isCLIM' and ChannelEventStatus flag ECLIM will be set.

Software KILL function controlled by the bit 'KILena' of the ChannelControl word:

KILL-enable = 1:	Voltage will be switched off permanently without ramp. ChannelEventStatus flag ECLIM will be set.
KILL-enable = 0:	Voltage will be switched off without ramp. If the output voltage arrives at 0 V the ramping to set voltage will be restarted automatically. ChannelStatus flag 'isCLIM' and ChannelEventStatus flag ECLIM will be set.

6.5.2.13 Supply24 (module read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read-	1	0x1104				
HV board write access	0	0x1104	Supply24			
Notes: Supply24 DATA_0 to DATA_3 [V] R4						

An 'out of range error' (see DCP group access: General status) will be generated if deviation of voltage is more than ±10%.

6.5.2.14 Supply5 (module read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read-	1	0x1105				
HV board write access	0	0x1105	Supply5			
Notes: Supply5 DATA_0 to DATA_3 [V] R4						

An 'out of range error' (see DCP group access: General status) will be generated if deviation of voltage is more than ±5%.

6.5.2.15 BoardTemperature (module read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read-	1	0x1106				
HV board write access	0	0x1106	BoardTemperature			
Notes: BoardTemperature DATA_0 to DATA_3 [°C] R4						

An 'out of range error' (see group access: General status) will be generated if the temperature is higher than +55°C.

6.5.2.16 Threshold to arm the errors detection (module write / read- write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1107	ThresholdArmErrorDetection			
master read-	1	0x1107				
HV board write access	0	0x1107	ThresholdArmErrorDetection			
Notes: ThresholdArmErrorDetection DATA_0 to DATA_3 [%] R4						

Factory setting for different kinds of HV modules is between 1V and to VO max/10 in percent to the nominal voltage of the channel.

The arming of the error detection is started while the actual voltage exceeds these value which has been stored before.

Exception: At the start of a ramp from zero the firmware evaluates that the feedback control will look in. If not, because the channel has a short or the hardware current limit is near to zero, then the channel will be switched off and a current error will be generated before the actual voltage is exceeding these threshold.

6.5.2.17 Serial number (module read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read-	1	0x1200				
HV board write access	0	0x1200	SerialNumber			
Notes: SerialNumber DATA_0 to DATA_3 UI4						

serial number e.g. 471212

6.5.2.18 Firmware release (module read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read-	1	0x1201				
HV board write access	0	0x1201	FrimwareRelease			
Notes: FirmwareRelease DATA_0 to DATA_3 UI1[4]						

release e.g. 01.00.00.00

6.5.2.19 Bit rate (module write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master read-	1	0x1202		
HV board write access	0	0x1202	BitRate	
Notes: BitRate DATA_0 to DATA_1 [kbit/s] UI2				

Following bit rates are possible: 20, 50, 100, 125, 250 kbit/s

The new bit rate gets active after RESET or POWER OFF/ON. The bit rate of all modules in the system must be the same before a RESET or POWER/ON is made.

- The bit rate is set to 250 kbit/s ex works.
- Invalid bit rates will be ignored and the bit 'Input error' of the will be set.
- A correct write access storing the information permanently if a NMT stop has been sent before.

6.5.2.20 Firmware Name (module read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_4/5	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x1203	NameOfFirmware				
master read-	1	0x1203					
HV board write access	0	0x1203	NameOfFirmware				
Notes: NameOfFirmware DATA_0 to DATA_3 [ASCII] BSTR							

BSTR	Description
“E16D0”	EDS 16 channel per board, distributor module, range of Vmax from VO max to (VO max - 1kV)
“E16D1”	EDS 16 channel per board, distributor module
“E08C0”	EHS 8 channel per board, common GND module
“E08F0”	EHS 8 channel per board, floating GND module
“E08F2”	EHS 8 channel per board, floating GND module, two current measurement ranges
“E08F7”	EHS 8 channel per board, cascaded floating GND channels
“E08C2”	EHS 8 channel per board, common floating GND module, two current measurement ranges
“E16C1	EHS 16 channel per board or 32 channels per module, common GND module
“E24D1”	EDS 24 channel per board, distributor module
“E24D3”	EDS 24 channel per board, distributor module
“E04B0”	EBS 4 channel per board, bipolar distributor module
“E08B0”	EBS 8 channel per board, bipolar distributor module
“E12B0”	EBS 12 channel per board, bipolar distributor module
“N06C2”	NHS NIM 6 channel module, common GND module, two current measurement ranges
“MICC”	MICC Multi channel Interface Crate Controller is a remote control interface for MMC Crates
“MICP”	MICP Multi channel Interface Crate PHQ Controller is a remote control interface for MMC Crates
“H101C0”	HPS 19”, 1 channel HV Power Supply (300W, 800W)
“H101C1”	HPS 19” 1 channel HV Power Supply 1.5kW - 10kW
“H201C0”	HPS compact 1channel HV Power Supply (350W)

6.5.2.21 ADC SamplesPerSecond SPS (module write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1204	SamplesPerSecond	
Master read-	1	0x1204		
HV board write access	0	0x1204	SamplesPerSecond	
Notes: SamplesPerSecond DATA_0 to DATA_1 [SPS] UI2 (possible SPS are 500, 100, 60, 50, 25, 10 and 5)				

Adjusts the number of averages of the programmable ADC filter of the HV modules. Possible values are 500, 100, 60 and 50 SPS. Notch should be set with 60 SPS using a 110V line with 60Hz and 50 SPS using a 230V line with 50Hz in order to improve the common-mode rejection of these frequencies. However a SPS value of the ADC will increase the main loop time by 4 • 1/SPS for devices “E08F0”, “E08F2” (see 6.5.2.20) respectively by 4 • 1/SPS multiplied with the number of channels for device “E16D0”, “E08C0” (see 6.5.2.20).

Factory settings: E16D0, E08C0, E16C1, E08F0: 500 SPS

E08F2, E08C2: 50 SPS.

6.5.2.22 DigitalFilter (module write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
master write	0	0x1205	NumberOfSteps	
master read-	1	0x1205		
HV board write access	0	0x1205	NumberOfSteps	
Notes: NumberOfSteps DATA_0 to DATA_1 [Steps] UI2 (possible steps are 1, 16, 64, 256,512 and 1024)				

The digital filter in the firmware of the processor reduces the white noise of the analog values of channel VoltageMeasure, channel CurrentMeasure. The digital filtering gives the possibility to get a higher precision and to react fast on changes of the measured values. The filter is not used during a voltage ramp. The filter is restarted after a significant change of the signal.

Factory settings: 64

6.5.2.23 ChannelNumber (module read access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read-	1	0x1208				
HV board write access	0	0x1208	ChannelNumber			
Notes: ChannelNumber DATA_0 to DATA_3 UI4						

6.5.2.24 ArticleDescription (module read access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_5	DATA_4	DATA_3	DATA_2	DATA_1	DATA_0
master read-	1	0x1209						
HV board write access	0	0x1209	ArticleDescription					
Notes: ArticleDescription DATA_0 to DATA_3 UI4								

This register returns the module article description. Depending on the length of the article description, multiple CAN messages may be sent. The description is terminated by a zero character.

6.5.2.25 ModuleOption (module read access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master read-	1	0x1280				
HV board write access	0	0x1280	ModuleOption			
Notes: ModuleOption DATA_0 to DATA_3 UI4						

The requested value of the module option is not valid when all bits are set to '1'!

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
EDCP	–	–	–	–	HVBPM	CLIM	VLIM
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
INHIBIT	RELAY	FRAMP	–	–	–	–	–
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
–	–	–	–	–	–	–	–
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
–	–	–	–	–	–	–	–

BIT	OPTION	DESCRIPTION /SPECIFICATION
Bit26	HVBM	HV boards per (CAN nodes) module
Bit25	CLIM	hardware current limit
Bit24	VLIM	hardware voltage limit
Bit23	INHIB	external INHIBIT signals
Bit22	RELY	discharge relay
Bit21	FRMP	fast ramp

6.5.2.26 ModuleOptionSpec (module read access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_4	DATA_3	DATA_2	DATA_1	DATA_0
master read-	1	0x1290	DATA_4	DATA_3	DATA_2	DATA_1	
HV board write access	0	0x1290	ModuleOption				Spec
Notes: ModuleOption Specfication			DATA_1 to DATA_4 DATA_0			UI4 UI1	

The requested value of the module option specification is not valid or do not exist when all bits are set to '1' or '0'!

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
EDCP	–	–	–	–	HVBPM	CLIM	VLIM
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
INHIBIT	RELAY	FRAMP	–	–	–	–	–
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
–	–	–	–	–	–	–	–
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
–	–	–	–	–	–	–	–

To request a specification the corresponding bit of the module option word has to be set to '1'.

Specification:	fast ramp	1	25% of VoltageNominal
		2	50% of VoltageNominal
		3	75% of VoltageNominal

Gibt es eine "4" für 100%??

6.5.2.27 ModuleCommMode (module write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
HV board write access	0	0x12a0	ModuleCommMode	
Notes: ModuleOption		DATA_0 to DATA_3	UI2	

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
–	–	–	–	–	–	–	–
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
–	–	–	–	–	–	–	FAST

Bit		Level	Description
Bit0	FAST	1	Fast communication mode (supported from isegHVOPCServer, isegCANHVControl)
		0	common mode

6.5.3 EDCP Group Accesses

The Multi Channel CAN module offers an extended and flexible range of group functions. There exist both predefined (so called fix) groups and variable groups.

Each group definition consists of 2 words each of 16 bits. In fix groups these 2 words are the value to be set into all channels (in float format) or they are a logical information. In variable groups one word carries the information about type and characteristics of the goup, the other word carries the information about the members of the group or gives an overview about a selected situation in all channels.

Four different grouptypes for variable groups have been established:

- Set group
- Status group
- Monitoring group
- Trip group

6.5.3.1 Set group

Set groups will be used in order to set channels to a same value, which happen to carry the identical channel value. Therefore within the group following will be defined:

- Member of the group: Each member will be activated in the channel setting list ChSetLst.
- Type of the group: Set group type TypeSet.
- Channel characteristics: Coding of characteristics, which have to be set commonly.
- Control mode: Divides between a one-time setting of the slave channel property and a permanently copying of the Master channel's property to the slave channels.
- Master channel: Number of the channel, which characteristics will be transferred to the other channels. Is just necessary for Set groups which set a value.
  If functions have to be initialized e.g. start of ramp then there is no Master channel.

EDCP frame:

Access	DATA_DIR	DATA_ID	NBR	OFFSET	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2000	Nx	Ox	ChSetLst		TypeSet	
master group read-	1	0x2000	Nx	Ox				
HV board write access	0	0x2000	Nx	Ox	ChSetLst		TypeSet	

Notes:

Nx	Group number		0 ... 31
Ox	Channel member offset		0, 16, 32 ... too access up to 255 channels
ChSetLst	DATA_2 to DATA_3	ChannelSettingList	members 0x1 ... 0xffff UI2
TypeSet	DATA_0 to DATA_1	TypeSet	UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
TYPE1	TYPE0	res	res	res	res	res	MOD0
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
SET3	SET2	SET1	SET0	MCH3	MCH2	MCH1	MCH0

TYPE1	TYPE0	Value	
0	0	SetGroupType	Group is defined as Set group

MOD0	Value	
0	0	The group function is done one time
1	1	The group function is done permanently

SET3	SET2	SET1	SET0	Value	
0	0	0	1	SetVset	Copy Vset from MCH to all members
0	0	1	0	SetIset	Copy Iset from MCH to all members
0	1	0	0	SetVbnds	Copy Vbounds from MCH to all members
0	1	0	1	SetIbnds	Copy Ibounds from MCH to all members
1	0	1	0	SetOn	Switch ON/OFF all members depending on setON in MCH
1	0	1	1	SetEmrgCutOff	Switch OFF all members (Emergeny OFF)
1	1	1	1	Cloning	Set all properties of members like MCH properties (in preparation)

MCH3	MCH2	MCH1	MCH0	Value	
0	0	0	0	0	1: Channel 0 is MasterChannel MCH
0	0	0	1	1	1: Channel 1 is MasterChannel MCH
...	...	...	...	...	...
1	1	1	1	15	1: Channel 15 ist MasterChannel MCH

6.5.3.2 Status group

Status groups are used to report the status of a single characteristic of all channels simultaneously. No action is foreseen. Therefore within the group following has to be defined:

- Members of the group: Each member will be activated in the channel status list ChStatLst.
- Type of the group: Status group type TypeStat
- Channel characteristics: Coding of characteristics which is to be reported.

EDCP frame:

Access	DATA_DIR	DATA_ID	NBR	OFFSET	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2000	Nx	Ox	ChStatList		TypeStat	
master group read-	1	0x2000	Nx	Ox				
HV board write access	0	0x2000	Nx	Ox	ChStatList		TypeStat	

Notes:

Nx	Group number	0 ... 31
Ox	Channel member offset	0, 16, 32 ... too access up to 255 channels
ChStatLst	DATA_2 to DATA_3 ChannelStatusList	members 0x1 ... 0xffff UI2
TypeStat	DATA_0 to DATA_1 TypeStatus	UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH15	CH14	CH13	CH12	CHST11	CHST10	CHST9	CHST8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CHST7	CHST6	CHST5	CHST4	CHST3	CHST2	CHST1	CHST0

ChannelStatusList

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
TYPE1	TYPE0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
STAT3	STAT2	STAT1	STAT0	Reserved	Reserved	Reserved	Reserved

TypeStatus

TYPE1	TYPE0	Value	
0	1	StatusGroupType	Group will be defined as Status group

SET3	SET2	SET1	SET0	Value	
0	0	1	1	ChkIsOn	check channel Status.isON (is on)
0	1	0	0	ChkIsRamping	check channel Status.isRAMP (is ramping)
0	1	1	0	ChkIsControlledCurrent	check channel Status.isCC (is current control)
0	1	1	1	ChkIsControlledVoltage	check channel Status.isCV (is voltage control)
1	0	1	0	ChkIsCurrentBounds	check channel Status.isCBNDs (is current bounds)
1	0	1	1	ChkIsVoltageBounds	check channel Status.isVBNDs (is voltage bounds)
1	1	0	0	ChkIsExternalInhibit	check channel Status.isEINH (is external inhibit)
1	1	0	1	ChkIsTrip	check channel Status.isTRIP(is trip)
1	1	1	0	ChkIsCurrentLimit	check channel Status.isCLIM (is current limit exceeded)
1	1	1	1	ChkIsVoltageLimit	check channel Status.isVLIM (is voltage limit exceeded)

6.5.3.3 Monitoring group

Monitoring groups are used to observe a single characteristic of selected channels simultaneously and in case of need take action. Therefore the group has to be defined:

- Members of the group: Each member will be activated in the channel monitoring list ChMonLst.
- Type of the group: Monitoring group type TypeMon
- Channel characteristics: Coding of characteristics which is to be monitored.
- Control mode: Coding of the control function, i.e. which kind of change in the group-image shall cause a signal.
- Activity: Define which activity has to happen after the event.

EDCP frame:

Access	DATA_DIR	DATA_ID	NBR	OFFSET	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2000	Nx	Ox	ChMonLst		TypeMon	
master group read-	1	0x2000	Nx	Ox				
HV board write access	0	0x2000	Nx	Ox	ChMonLst		TypeMon	

Notes:

Nx	Group number	0 ... 31	
Ox	Channel member offset	0, 16, 32 ... too access up to 255 channels	
ChMonLst	DATA_2 to DATA_3 ChannelMonitoringList	members 0x1 ... 0xffff	UI2
TypeMon	DATA_0 to DATA_1 TypeMonitoring		UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

ChMonLst

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
TYPE1	TYPE0	ACT1	ACT0	res	res	res	MOD0
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
MON3	MON2	MON1	MON0	Reserved	Reserved	Reserved	Reserved

TypeMon

TYPE1	TYPE0	Value	
1	0	MonitoringGroupType	Group will be defined as Monitoring group

ACT1	ACT0	Value	
0	0	0	No special action ; EventGroupStatus[grp] will be set
0	1	1	Ramp down of group EventGroupStatus[grp] will be set
1	0	2	Shut down group without ramp; EventGroupStatus[grp] will be set
1	1	3	Shut down module without ramp; EventGroupStatus[grp] will be set

MOD0	Value	
0	0	event will happen if at least one Channel == 0
1	1	event will happen if at least one Channel == 1

MON3	MON2	MON1	MON0	Value	
0	0	1	1	MonitorIsOn	monitor channel Status.isON (is on)
0	1	0	0	MonitorIsRamping	monitor channel Status.isRAMP (is ramping)
0	1	1	0	MonitorIsControlledCurrent	monitor channel Status.isCC (is Constant Current)
0	1	1	1	MonitorIsControlledVoltage	monitor channel Status.isCV (is Constant Voltage)
1	0	1	0	MonitorIsCurrentBounds	monitor channel Status.isCBNDs (is Current Bounds)
1	0	1	1	MonitorIsVoltageBounds	monitor channel Status.isVBNDs (is Voltage Bounds)
1	1	0	0	MonitorIsExternalInhibit	monitor channel Status.isEINH (is External Inhibit)
1	1	0	1	MonitorIsTrip	monitor channel Status.isTRIP (is Trip)
1	1	1	0	MonitorIsCurrentLimit	monitor channel Status.isCLIM (is Current Limit exceeded.)
1	1	1	1	MonitorIsVoltageLimit	monitor channel Status.isVLIM (is Voltage Limit exceeded.)

6.5.3.4 Delayed Trip group

Trip timeout groups are necessary to keep the timing for the time controlled delayed Trip function and to define the action which has to happen after a Trip.

Therefore in the group following will be defined:

- Members of the group: Each member will be activated in a word channel trip timeout list ChTrpTotLst.
- Type of the group: Time out group type TypeTime
- Activity: Define which activity has to happen after time controlled Trip
- Timeout: Coding of Timeout-time as integer value.

Timeout groups have to stay unchanged for the whole time as long they are used.
An overwriting will cause the definition of a new group. An overlay of the channels of multiple Trip groups is not allowed.

EDCP frame:

Access	DATA_DIR	DATA_ID	NBR	OFFSET	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2000	Nx	Ox	ChTrpTotLst		TypeTime	
master group read-	1	0x2000	Nx	Ox				
HV board write access	0	0x2000	Nx	Ox	ChTrpTotLst		TypeTime	

Notes:

Nx	Group number	0 ... 31
Ox	Channel member offset	0, 16, 32 ... too access up to 255 channels
ChTrpTotLst	DATA_2 to DATA_3 ChannelTripTimoutList	members 0x1 ... 0xffff UI2
TypeTime	DATA_0 to DATA_1 TypeTimeOut	UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

ChTrpTotLst

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
TYPE1	TYPE0	ACT1	ACT0	TOT11	TOT10	TOT9	TOT8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
TOT7	TOT6	TOT5	TOT4	TOT3	TOT2	TOT1	TOT0

TypeTime

TYPE1	TYPE0	Value	
1	1	TimeOutGroupType	Group will be defined as Timeout group

ACT1	ACT0	Action	
0	0	0	No special action; EventGroupStatus[grp] will be set.
0	1	1	Ramp down group with ramp; EventGroupStatus[grp] will be set
1	0	2	Shut down the group without ramp; EventGroupStatus[grp] will be set
1	1	3	Shut down the module without ramp; EventGroupStatus[grp] will be set

INFORMATION

NOTE

TOT[11..0]:
Timeout-time in ms (8..4088ms) resolution is 8ms (different values to 8ms resolution will be rounded)

Set voltage of all channels (group write access)
EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x2100	VoltageSetAllChannels			
Notes: VoltageSetAllChannels		DATA_0 to DATA_3 [V]		R4		

(see VoltageSet Single access also)

6.5.3.5 Request Temperatures and Supplies (group write access)

Message	DLC	DataID	Channel	Data	Data	Data	Data	Value
Request all Temperatures	2	20 01						
Temperature 0	7	20 01	00	41	EF	0D	B0	29.9 °C
Temperature 1	7	20 01	01	41	ED	66	30	29.7 °C
Temperature 2	7	20 01	02	41	EF	0D	B0	29.9 °C
Request all Measured Supplies	2	20 02						
Positive supply external +24	7	20 02	00	41	BE	75	98	23,8 V
Negative supply external -24	7	20 02	01	C1	C0	00	00	-24 V
Logic supply external +5	7	20 02	02	40	A0	51	EC	5,01 V
Positive supply op-amp	7	20 02	03	41	40	00	00	12
Negative supply op-amp	7	20 02	04	C1	40	00	00	-12
Logic intern +5	7	20 02	05	40	A0	51	EC	4.99 V
Ligic intern +3.3	7	20 02	06	40	53	2E	1C	3.29 V
Reserved	7	20 02	07	00	00	00	00	0 (res)
Reserved	7	20 02	08	00	00	00	00	0 (res)

6.5.3.6 GroupVoltageLimit – OPTION (module read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_4	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x2005					
HV board write access	0	0x2005	Channel	VoltageMax			
Notes: HardwareVoltageLimit DATA_0 to DATA_3 [%] R4 VoltageMax Channel							

6.5.3.7 GroupCurrentLimit – OPTION (module read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_4	DATA_3	DATA_2	DATA_1	DATA_0
master read -	1	0x2006					
HV board write access	0	0x2006	Channel	CurrentMax			
Notes: HardwareVoltageLimit DATA_0 to DATA_3 [%] R4 CurrentMax Channel							

6.5.3.8 Set voltage of all channel (group write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x2101	VoltageSetAllChannels			
Notes: VoltageSetAllChannels		DATA_0 to DATA_3 [A]		R4		

(see CurrentSet Single access also)

6.5.3.9 Set current (– trip) of all channels (group write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master write access	0	0x2101	CurrentSetAllChannels			
Notes: CurrentSetAllChannels		DATA_0 to DATA_3 [A]		R4		

(see CurrentSet Single access also)

6.5.3.10 Set ON / OFF of all channels (group write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2200	SetOnOffAllChs			
master group read-	1	0x2200				
HV board write access	0	0x2200	SetOnOffAllChs			

Notes:

SetOnOffAllChs	DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment)	UI4
SetOnOffAllChs	DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment)	UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

SetOnOffAllChs	DATA_0 to DATA_1 for channel 0 to channel 15	UI2
CHm = 1	Channel ON	
CHm = 0	Channel OFF	

The SetOnOffAllChs represents a 32 bit field to control the channel property setON for each channel member of the bit field with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to setON for all channel members simultaneously with on instruction.

6.5.3.11 Set EMERGENCY of all channels (group write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2201	SetEmergencyAllChs			
master group read-	1	0x2201				
HV board write access	0	0x2201	SetEmergencyAllChs			

Notes:

SetEmergencyAllChs	DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment)	UI4
SetEmergencyAllChs	DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment)	UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

SetEmergencyAllChs DATA_0 to DATA_1 for channel 0 to channel 15 UI2

CHm = 1 Channel EMERGENCY set

CHm = 0 Channel EMERGENCY reset

The SetEmergencyAllChs represents a 32 bit field to control the channel property setEMCY for each channel member of the bit field with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to setEMCY for all channel members simultaneously with on instruction.

6.5.3.12 Event status voltage limit of all channels (group write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2202	EventStatusVLimitAllChs			
master group read-	1	0x2202				
HV board write access	0	0x2202	EventStatusVLimitAllChs			

Notes:

EventStatusVLimitAllChs	DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment)	UI4
EventStatusVLimitAllChs	DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment)	UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

EventStatusVLimitAllChs	DATA_0 to DATA_1 for channel 0 to channel 15	UI2
CHm = 1	Channel event status voltage limit	
CHm = 0	nothing	

The EventStatusVLimitAllChs represents a 32 bit field to control the channel property EVLIM for each channel with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to reset EVLIM for all channel members simultaneously with on instruction.

If the voltage limit was exceeded or an external over voltage occurs at the channel output (i.e. Output voltage > Set voltage) then the channel will be switched off and the according bit will be set. The error bits will be canceled and the voltage of the corresponding channel can be switched on again only after writing 'EventStatusVLimitAllChs' with the bits, which are corresponding to the channel errors are set to "1".

6.5.3.13 Event status current limit of all channels (group write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2203	EventStatusCLimitAllChs			
master group read-	1	0x2203				
HV board write access	0	0x2203	EventStatusCLimitAllChs			

Notes:

EventStatusCLimitAllChs	DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment)	UI4
EventStatusCLimitAllChs	DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment)	UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

EventStatusCLimitAllChs DATA_0 to DATA_1 for channel 0 to channel 15 UI2

CHm = 1 Channel event status current limit

CHm = 0 nothing

The EventStatusCLimitAllChs represents a 32 bit field to control the channel property ECLIM for each channel with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to reset ECLIM for all channel members simultaneously with on instruction.

The module responds to the exceeding of the hardware current limit which has been set in the channel in dependence on the according setKILena bit of module control as follows:

setKILena = 1: Voltage will be switched off permanently without ramp, green LED on front panel is off until a write of EventStatusCLimitAllChs with the bits, which are corresponding to the channel errors set to “1”. The error bits will be cancelled and the voltage of the corresponding channels can be switched on again.

setKILena = 0: HV modules without a current control E16D0, E16D1 and E08B0 will be switched off voltage without ramp, green LED on front panel is off. If the output voltage arrives at 0 V the ramping to set voltage will be started automatically again. The green LED again flash only after writing the EventStatusCLimitAllChs with the respective bits.

HV modules with a current control will not switch off high voltage and operate in constant current mode, green LED on front panel is off. The output current will be limited. The green LED flashes only after writing of EventStatusCLimitAllChs with the respective bits and removing of the limitation of current before.

6.5.3.14 Event status trip of all channels (group write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2204	EventStatusTrpAllChs			
master group read-	1	0x2204				
HV board write access	0	0x2204	EventStatusTrpAllChs			

Notes:

EventStatusTrpAllChs	DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment)	UI4
EventStatusTrpAllChs	DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment)	UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

EventStatusTrpAllChs	DATA_0 to DATA_1 for channel 0 to channel 15	UI2
CHm = 1	Channel event status trip	
CHm = 0	notihing	

The EventStatusTrpAllChs represents a 32 bit field to control the channel property ETRP for each channel with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to reset ETRP for all channel members simultaneously with on instruction.

If the output current exceeds the programmed current trip value then the corresponding bits will be set:

setKILena = 1: Voltage will be switched off permanently without ramp, green LED on front panel is off until a write of EventStatusTrpAllChs with the bits, which are corresponding to the channel errors set to “1”. The error bits will be cancelled and the voltage of the corresponding channels can be switched on again.

setKILena = 0: HV will not be switched but the green LED on front panel is off. The output current will be limited if there is a current control. The green LED flashes only after writing of EventStatusTrpAllChs with the respective bits and removing of the limitation of current before.

6.5.3.15 Event status inhibit of all channels (group write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2205	EventStatusInhAllChs			
master group read-	1	0x2205				
HV board write access	0	0x2205	EventStatusInhAllChs			

Notes:
EventStatusInhAllChs DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) UI4
EventStatusInhAllChs DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment) UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

EventStatusInhAllChs	DATA_0 to DATA_1 for channel 0 to channel 15 UI2
CHm = 1	Channel event status inhibit
CHm = 0	notihing

The EventStatusInhAllChs represents a 32 bit field to control the channel property ETRP for each channel with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to reset ETRP for all channel members simultaneously with on instruction.

Voltage will be switched off permanently without ramp, if the INHIBIT is active, the green LED on front panel is off. When the INHIBIT is going back from active to passive state then the INHIBIT flag have to be erased by write of the EventStatusInhAllChs before the voltage can be switched on again. The INHIBIT flags are reset with set of the corresponding channel bit to “1”.

6.5.3.16 Set ON / OFF channels extender (group write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2280	SetOnOffChsExtender			
master group read-	1	0x2280				
HV board write access	0	0x2280	SetOnOffChsExtender			

Notes:
SetOnOffAllChs DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) UI4
SetOnOffAllChs DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment) UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
CH63	CH62	CH61	CH60	CH59	CH58	CH57	CH56
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
CH55	CH54	CH53	CH52	CH51	CH50	CH49	CH48
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH47	CH46	CH45	CH44	CH43	CH42	CH41	CH40
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CH39	CH38	CH37	CH36	CH36	CH34	CH33	CH32

SetOnOffAllChs DATA_0 to DATA_1 for channel 0 to channel 15 UI2

CHm = 1 Channel ON

CHm = 0 Channel OFF

The SetOnOffChsExtender represents a 32 bit field to control the channel property setON for each channel member of the bit field with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to setON for all channel members simultaneously with on instruction.

6.5.3.17 Set EMERGENCY channels extender (group write- / read-write access)

EDCP frame:

Access	DATA_DIR	DATA_ID	DATA_3	DATA_2	DATA_1	DATA_0
master group write	0	0x2201	SetEmergencyChsExtender			
master group read-	1	0x2201				
HV board write access	0	0x2201	SetEmergencyChsExtender			

Notes:
SetEmergencyChsExtender DATA_0 to DATA_3 for channel 0 to 31 (channel 16 to 31 are reserved at the moment) UI4
SetEmergencyChsExtender DATA_2 to DATA_3 for channel 16 to channel 31 (reserved at the moment) UI2

Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24
CH63	CH62	CH61	CH60	CH59	CH58	CH57	CH56
Bit23	**Bit22**	**Bit21**	**Bit20**	**Bit19**	**Bit18**	**Bit17**	**Bit16**
CH55	CH54	CH53	CH52	CH51	CH50	CH49	CH48
Bit15	**Bit14**	**Bit13**	**Bit12**	**Bit11**	**Bit10**	**Bit09**	**Bit08**
CH47	CH46	CH45	CH44	CH43	CH42	CH41	CH40
Bit07	**Bit06**	**Bit05**	**Bit04**	**Bit03**	**Bit02**	**Bit01**	**Bit00**
CH39	CH38	CH37	CH36	CH36	CH34	CH33	CH32

SetEmergencyChsExtender DATA_0 to DATA_1 for channel 0 to channel 15 UI2

CHm = 1 Channel EMERGENCY set

CHm = 0 Channel EMERGENCY reset

The SetEmergencyChsExtender represents a 32 bit field to control the channel property setEMCY for each channel member of the bit field with one bit in the bit-field. The data point is one of the EDCP group functions with advantage to setON for all channel members simultaneously with on instruction.

6.5.4 Important DCP Module Accesses

6.5.4.1 General status (group write- / read-write / active access)

DCP frame:

Access	EXT_INSTR	DATA_DIR	DATA_ID	DATA_1	DATA_0
HV board active access	0	0	0xc0	GeneralStatus	Details
Notes: GeneralStatus DATA_1 UI1					

b15	b14	b13	b12	b11	b10	b9	b8
Save	KILLena/ HwVLnotLow	SPLYTMPgd	AvAd	Stbl	SFLPgd	noRamp	noSumErr
b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
INHB	BordTemp	res	res	VLIM	CLIM	RERR	TRP

Details DATA_0 UI1

XXX	XXX	XXX
Save	Save	save function bit stored permanently the current set values (takes some seconds ca. 10s)
KILLena	KillEnable	kill function bit
HwVLnotLow	HardwareVoltageLimitNotLow	hardware voltage limit is not to low bit, for device class 21 only
SPLYTMPgd	SupplyGoodTemperatureGood	supply good and board temperature good bit
AvAd	AverageAdjust	average and fine adjustment bit
SFLPgd	SaftyLoop	safety loop bit
noRamp	noRamp	flag to display that no voltage is ramping
noSumErr	NoSumError	displays that there has been built a sum error flag by VLIM&ILIM&TRP over all channels
INHB	Inhibit	an external INHIBIT at least one of the channels (device class 25)
BoardTemp	BoardTemperatureGood	board temperature is good
VLIM	VoltageLimit	hardware voltage limit has been exceeded
CLIM	CurrentLimit	hardware current limit has been exceeded
RERR	RegulationError	regulation error, for device class 21 only
TRP	Trip	voltage or current trip
res	reserved	

XX	XX
Save=0	no write access to EEPROM
Save=1	store all set values to EEPROM (time to save ca. 10s) for device classes 24 and 25 only
KILLena=0	kill function disable
KILLena = 1	kill function enable, for device classes 21 only
HwVLnotLow = 0	HW Vlimit voltage limit is to low, it is not possible to switch on the HV, reset by write with HwVLToLow flag is set to “1”
HwVLnotLow = 1	HW Vlimit in proper range
SPLYTMPgd = 0	supply voltages are out of range or module temperature > 55°C
SPLYTMPgd = 1	supply voltages are in range and module temperature ≤ 55°C
AvAd = 0	fine adjustment and average of voltage, current measurement OFF
AvAd = 1	fine adjustment and average of voltage, currentmeasurement ON
Stbl = 0	all channels are stable with program ADC filter frequency fN. (ADC conversion time =1/fN, see ‘Set ADC filter frequency‘, default fN=50 Hz)
Stbl = 1	at least one channel is ramping Vo or not yet stable after ramping (ramping - with ADC filter frequency fN=100 Hz)
SFLPgd = 0	safety loop is broken -VO bas been shut off, reset by a write of the ‘General status‘ with sloop flag is set to “1”
SFLPgd = 1	safety loop is closed
noRamp = 0	VO is ramping in at least one channel
noRamp = 1	no channel is ramping
noSumErr = 0	voltage limit, current limit or trip has been exceeded in at least one of the channels (error)
noSumErr = 1	status channel flags v & c & t = 0 for all channels (no errors)
INHB = 0	no external INHIBIT signal
INHB = 1	external INHIBIT signal
BoardTemp = 0	temperature ≤ 55°C
BoardTemp = 1	temperature > 55°C
VLIM=0	hardware voltage limit hasn’t been exceeded
VLIM=1	hardware voltage limit has been exceeded
CLIM=0	hardware current limit hasn’t been exceeded
CLIM=1	hardware current limit has been exceeded
RERR=0	hardware current hasn’t been exceeded
RERR=1	voltage has been exceeded
TRP=0	no trip
TRP=1	voltage or current trip

If one of the bits noHwVLtoLow, SPLYTMPgd, SFLPgd, noSumErr in the modul access “General status module” has not been set, the module will send this access as an active error message with higher priority (ID9=0). An additional 2nd data byte offers more information about the NoSumError flag of the first byte. OPC

Example of an active error message

access	identifier	length code	DATA_ID	DATA_1	DATA_0
HV board active access	0x180	3	0xc0	0x57	0x01

TRP=1 noSumErr=0 etc.

6.5.4.2 Log-on / Log-off Front-end device at superior layer (module active- / write access)

DCP frame:

Access	DATA_DIR	DATA_ID	DATA_1	DATA_0
HV board active access	1	0xD8	GeneralStatus	DeviceClass
master write access	0	0xD8	LogOnOff	
Notes: GeneralStatus DATA_1 – refer chapter 4. UI1 DeviceClass DATA_0 UI1				

device class EDCP	device class DCP	label	firmware	description	associated serial numbers
21	0	EDS	E16D0_xxx E16D1_xxx E24D1_xxx	EDS 16 channels per PCB EDS 16 channels per PCB EDS 24 channels per PCB	471xxx / 71xxxx
22	-	HPS / LPS	H101C0_5xx	HPS 19”, 1 channel HV Power Supply (300W, 800W)	68xxxx / 70xxxx
23	-	HPS / LPS	H201C0_2xx	HPS compact,1 channel HV Power Supply (350W)	68xxxx / 70xxxx
24 24 25 25	6 6 7 7	EHS/EMS/ELS	E08C0_xxx	ExS 8 channel per PCB, standard common GND	73xxxx 73xxxxx 74xxxx 74xxxxx
25	7	EHS/EMS/ELS	E08F0_xxx	ExS 8 channel per PCB, standard, floating GND	474xxx
26	2	EHS/EMS/ELS	E08F2_xxx	ExS 8 channel per PCB, floating GND 2 ranges for measurement of current	72xxxx 72xxxxx
27	-	EHS/EMS/ELS	E08C2_xxx	ExS 8 channel per PCB, common floating GND 2 ranges for measurement of current	78xxxx 78xxxxx
41	-	MICC	MICC_3xx	MICC Multichannel Interface Crate Controller for MMC Crates	458xxx
42	-	MICP	MICP_3xx	MICP Multichannel Interface Crate PHQ Controller for MMC Crates	458xxx
60	-	HPS	H101C1_1xx	HPS 19”, 1 channel HV Power Supply (1.5kW – 10 kW)	90xxxxx
70	-	EHS	E16C1_1xx	ExS 16 channels per PCB or 32 channels per module	79xxxx 79xxxxx

LogOnOff	DATA_1=1 superior layer send a “Log-on” at Front-end device to registration DATA_1=0 superior layer send “Log-off” to Front-end device xxx and xxxx are running numbers	UI1

After POWER ON the Front-end device - up to a number of two per module - will give this module access cyclically on the bus (ca. 1 sec). If a controller of superior layer identifies this access then it is possible to register this as a Front-end device and is possible to address it with FE_ADR. (see also description 11bit-Identifier)

After the successful registration the Front-end device will not send further ‘Log-on” accesses as long as:

- it receives accesses from the external CAN Bus in periods shorter than one minute or
- until the superior controller will send a ‘Log-off” access to the Front-end device.

6.5.5 Events

The module provides an extended event collecting logic. This is necessary to monitor extraordinary events and forward them to the host.

6.5.5.1 Channel events

These event-bits in the channel event status register are related to mask bits in the channel event mask register. With help of an AND function (bit-wise) between an event bit and the according mask bit a result only occurs where the mask bit has been set. A following logic OR function of all of these results leads to the event status of the channels.

ModuleEventChannelStatus[ch] = (ChannelEventStatus.EVLIM[ch] AND ChannelEventMask.MEVLIM[ch]) OR
(ChannelEventStatus.ECLIM[ch] AND ChannelEventMask.MECLIM[ch]) OR
(ChannelEventStatus.ETRP[ch] AND ChannelEventMask.METRP[ch]) OR
(ChannelEventStatus.EEINH[ch] AND ChannelEventMask.MEEINH[ch]) OR
(ChannelEventStatus.EVBNDs[ch] AND ChannelEventMask.MEVBNDs[ch]) OR
(ChannelEventStatus.ECBNDs[ch] AND ChannelEventMask.MECBNDs[ch]) OR
(ChannelEventStatus.ECV[ch] AND ChannelEventMask.MECV[ch]) OR
(ChannelEventStatus.ECC[ch] AND ChannelEventMask.MECC[ch]) OR
(ChannelEventStatus.EEMCY[ch] AND ChannelEventMask.MEEMCY[ch]) OR
(ChannelEventStatus.EEOR[ch] AND ChannelEventMask.MEEOR[ch]) OR
(ChannelEventStatus.EOn2Off[ch] AND ChannelEventMask.MEOn2Off [ch]) OR
(ChannelEventStatus.EIER[ch] AND ChannelEventMask.MEIER[ch])
ch={0..n}

The status of all channel events is collected in the register EventChannelStatus of the module items.

For a selection or filtering of the channel events a related mask register has been provided (ModuleEventChannelMask). With help of the AND or OR function (see channel) the event active signal of the channels EventChannelActive will be generated:

EventChannelActive = (EventChannelStatus[0] AND EventChannelMask[0]) OR
(EventChannelStatus[1] AND EventChannelMask[1]) OR
...
(EventChannelStatus[n] AND EventChannelMask[n])

6.5.5.2 Group events (in preparation)

Like written before groups are also able to generate Events. These events will be collected in the status word EventGroupStatus of the GroupData. With help of the mask register EventGroupMask the event active signal of the groups EventGroupActive will be generated.

EventGroupActive	=	(EventGroupStatus[0] AND EventGroupMask[0]) OR
		(EventGroupStatus[1] AND EventGroupMask[1]) OR
		...
		(EventGroupStatus[23] AND EventGroupMask[24])

6.5.5.3 Module events

With help of the NOT, AND or OR function the event active signal of the module EventModuleActive will be generated:

EventModuleActive	=	(NOT(ModuleEventStatus.ETMPngd) AND ChannelEventMask.METMPngd) OR
		(NOT(ModuleEventStatus.ESPLYngd) AND ChannelEventMask.MESPLYngd) OR
		(NOT(ModuleEventStatus.ESFLPngd) AND ModuleEventMask.MESFLPngd) OR

From both signals EventChannelActive and EventModuleActive the global event active signal of the module IsEventActive of the ModuleStatus register will be generated.

IsEventActive	=	(EventChannelActive OR EventGroupActive OR EventModuleActive

This global signal 'IsEventActive' triggers a fast message on the CAN bus with the DCP Module frame of General status.

Example: WIE WEIT GEHT DAS BEISPIEL? Sind das mehrere?

The event flag ECC of the ChannelEventStatus for channel 2 or the event flag EventTemperatureNotGood of the ModuleEventStatus should release a fast CAN frame:

- Channel[2].ChannelEventMask.Bit.MECC = 1
- Module.EventChannelMask.Bit.2 = 1

- Module.EventMask.Bit.METMPngd = 1

The signal isEvntActive is triggerd and release a fast CAN frame of General status when:

(Channel[2].ChannelEventStatus.Bit.ECC & Channel[2].ChannelEventMask.Bit.MECC & Module.ModuleEventChannelMask.Bit2

OR

Module.ModuleEventStatus.Bit.ETMPngd & Module.ModuleEventMask.Bit.METMPngd

OR

(Module.ModuleEventChannelStatus.Bit2 & Module.ModuleEventChannelMask.Bit2)

Fast CAN frame in case of Channel[2].ChannelEventStatus.Bit.ECC == 1:

0x190 3 0xc0 0x37 0x00 (ID=0x190, ID9=0; Len=3; DATA_ID=0xc0; Data=0x3700)

(Channel[2].ChannelEventStatus.Bit.ECC & Channel[2].ChannelEventMask.Bit.MECC)==1 ➜ ModuleEventChannelStatus.Bit2=1

Fast CAN frame in case of Module.ModuleEventStatus.Bit. ETMPngd == 1:

0x190 3 0xc0 0x17 0x40 (ID=0x190, ID9=0; Len=3; DATA_ID=0xc0; Data= 0x1740)

INFORMATION

NOTE

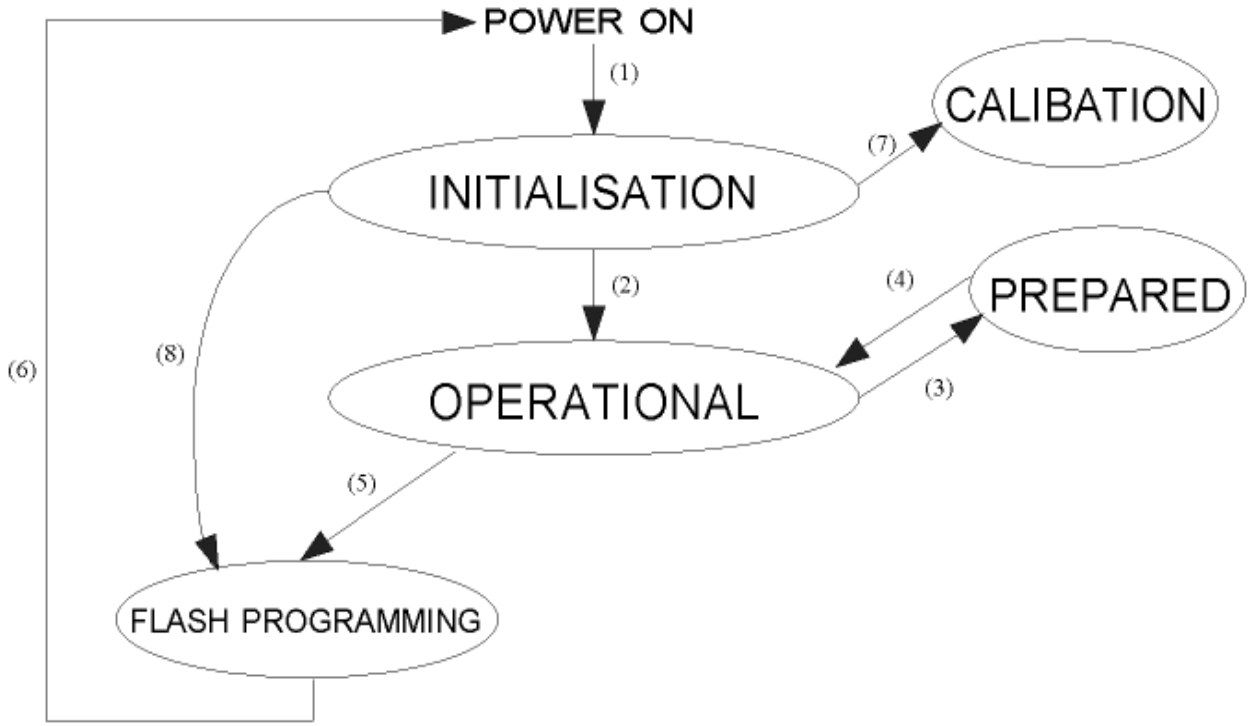
Please note that, a release of a fast CAN frame is different in handling depending on EDCP or DCP mode!

Appendix A – Shortcuts

BCD	binary coded decimal format
CAN	controller area network
Chm	channel m=0..15 (Teilweise war doch bis 64 beschrieben bei den Kanälen?)
CHN	channel
DCP	device control protocol
DATA_ID	data identifier of DCP
fN	first filter notch frequency
HV	High voltage
HW	hardware
Imeas	Actual current
Imax	Hardware current limit
IO max	Nominal current
Iset	Set current
Itrip	Trip current
ISO	International Standard Organization
LSB	least significant bit
MBR	channel members
MSB	most significant bit
NBR	group number
NMT	network management service
OSI	Open System Interconnect
PCB	printed circuit board
p/a	passive / active
SN.	serial number
UI1	unsigned character
SI1	signed character
UI2	unsigned short integer (16 bit)
UI4	unsigned integer (32 bit)
R4	float according to IEEE-754 single precision format
Vmeas	Actual voltage
Vmax	Hardware voltage limit
VO max	Nominal voltage
Vset	Set voltage
SW	software

Eventuell ein Abgleich mit dem SCPI Handbuch und den Beschreibungen unter 1.3

Appendix B – Diagram of operating modes



(1) The INITIALIZATION follows after the POWER ON reset of the device hardware. It can be differ between different device classes.

(2) The state OPERATIONAL will be obtained by the device itself if all initializations are ready or the state PREPARED runs in time out.

(3) NMT Stop switches the devices of the CAN segment into the state PREPARED. In this state the permanent settings of the devices can be changed (per device Bit rate, Set voltage, Set current, Ramp speed, General status, Threshold to arm the errors detection, Discharge relay configuration, CAN message configuration and additional the Bit rate as a broadcast massage).

(4) NMT Start takes the devices of the CAN segment back to the OPERATIONAL state.

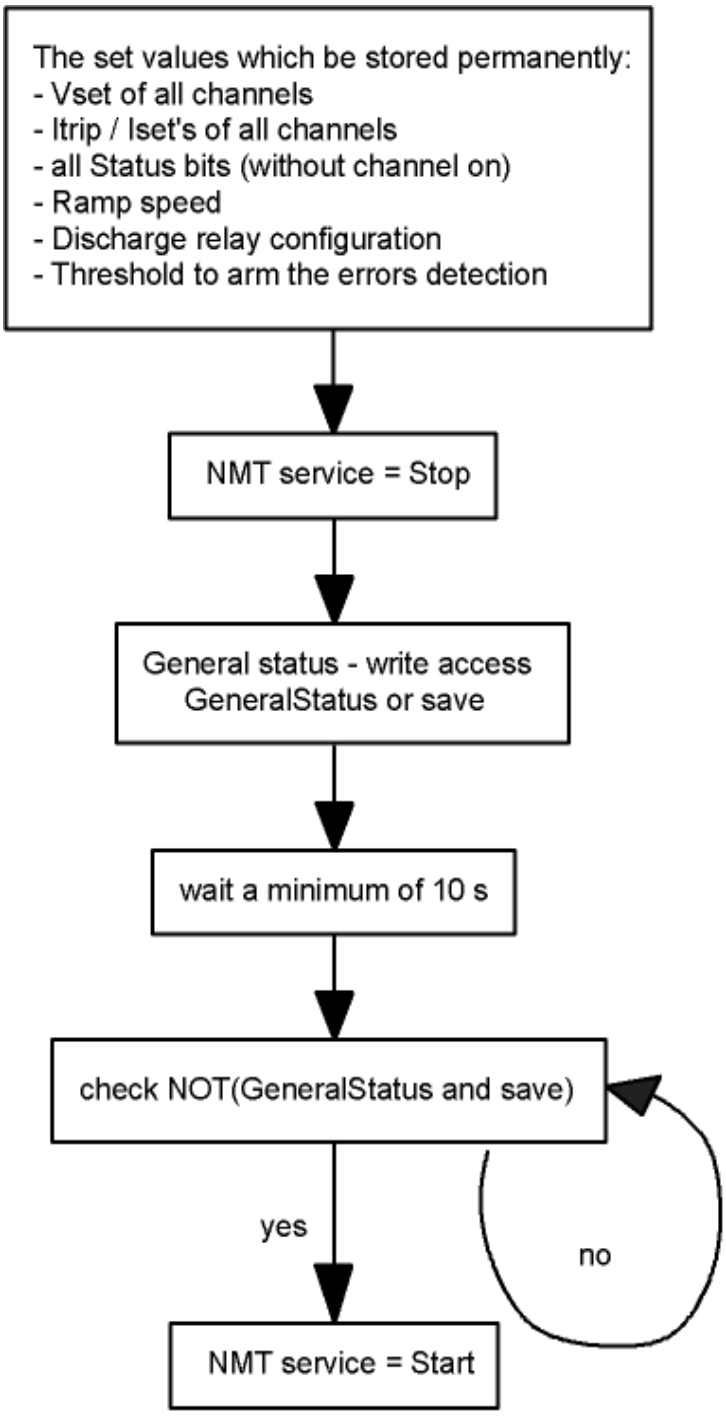
(5) With the special Flash programming access the device runs into the state FLASH PROGRAMMING. The high voltage will be switched off automatically before.

(6) The device will execute a POWER ON reset itself at the end of FLASH PROGRAMMING.

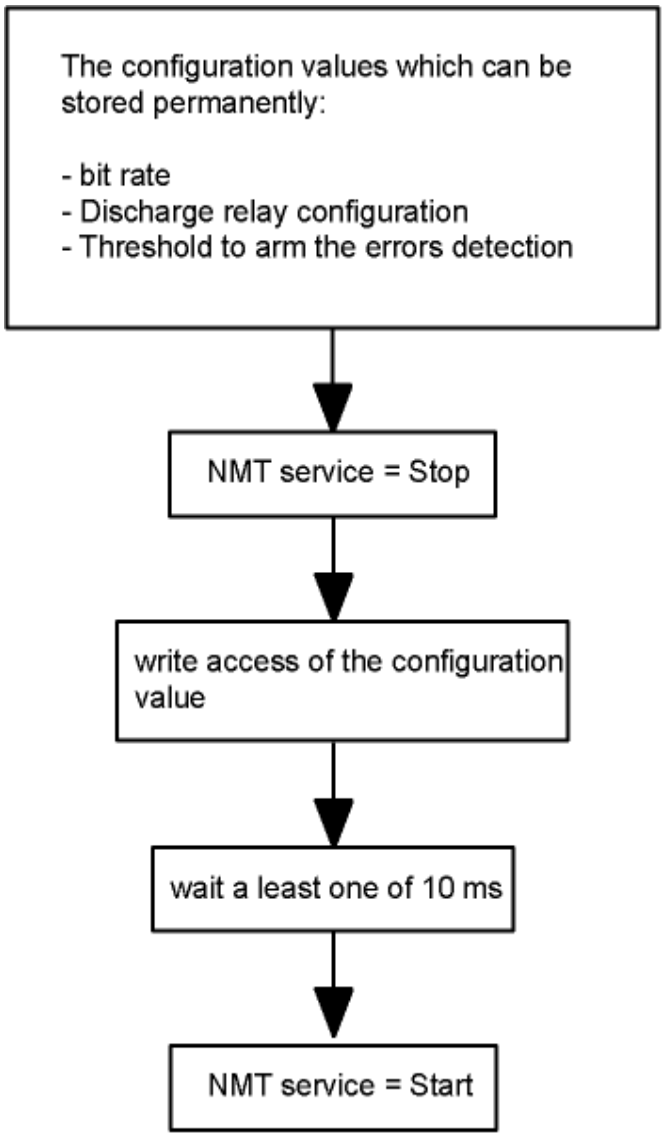
(7) The state CALIBRATION will be obtained by setting of the corresponding switches at the Calibration Crate.

(8) The state FLASH Programming will be obtained also if the corresponding switch at the Calibration Crate / Flash Programming Slot are set.

Appendix C – Programming flowchart to store the settings permanently with help of General state save bit



Appendix D – Programming flowchart to store the configurations of the module permanently with help of General state save bit



7 Manufacturer´s contact

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