Technical information
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CAN Interface Programmers Guide
for NHQ High Precision and Standard Modules

Document history

Version	Date	Major changes
2.0	20.09.2017	Relayouted documentation

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1. Device Control Protocol DCP

The communication between the controller and the module is realized according to the Device Control Protocol DCP, which has been designed for the use of multi-level hierarchical systems of instruments.

This protocol works according to the master slave principle. Therefore, the controllers which are on higher hierarchy level are always masters, while devices on lower hierarchy level are working as slaves.

For the case "controlling a HV device by a controlling computer", the controller will have the master function in this system, while the module (as a Front-end device with intelligence) will be the slave.

The data exchange between the controller and the Front-end (FE) device is working with help of data frames. These data frames consist of one direction bit DATA_DIR, one identifier byte DATA_ID and further data bytes. The direction bit DATA_DIR defines whether the data frame handles a write or read-write access. The DATA_ID carries the information about the type of the data frame and if necessary sub addresses (G0, G1). It is characterized by the first byte of the data frame with bit 7=1. The DATA_ID identifies the function of the module within the complex HV system.

In such systems with many hierarchical levels a single function of a single module can be addressed by using group controllers (GC). In this case additional data bytes with bit 7=0 are included in the data frame in front of the DATA_ID to submit the address of the GC and the FE.

DATA_DIR	DATA_ID Bit								Access
	7	6	5	4	3	2	1	0	
x	0	x	x	x	x	x	x	x	No DATA_ID
0	1	0	x	x	x	x	x	x	Write access on Front-end device
1	1	0	x	x	x	x	x	x	Read-write access on Front-end device (Request at Write)
0	1	1	x	x	x	x	G1	G0	Write access on group
1	1	1	x	x	x	x	G1	G0	Read-write access on group (Request at Write)
									G0, G1 sub address, only needed if group controller (GC) is used

These data frames correspond to a transfer in layer 3 (Network Layer) respectively layer 4 (Transport Layer) of the OSI model of ISO. The transmission medium is the CAN Bus according to the specification 2.0B and corresponding to level1 (Physical Layer) and level 2 (Data Link Layer).

The Device Control Protocol DCP has been matched to the CAN Bus according to specification CAN 2.0B. It is also possible to match according the OSI model to further transmission media (e.g. RS 232). Therefore the details of layer 1 and 2 are only addressed if absolutely necessary and where a confusion between functions of the Transport Layer and functions of the Data Link Layer can occur. The communication between the controller and a module on the same bus segment will be described as follows.

1.1 Function range

The following functionality is provided for the operation of the high voltage units via the CAN interface.

1.1.1 CAN-control mode

- Write function: set voltage; ramp speed; maximal output current (current trip); auto start
- Switch function: output voltage = set voltage, output voltage = 0
- Read function: set voltage; actual output voltage; ramp speed; actual output current; current trip; auto start ; hardware limits current and voltage; status

Front panel switches have priority over software control.

1.1.2 Manual control mode

While the unit is operating in manual control mode, only CAN read accesses are interpreted. Write accesses are accepted, but do not result into a change of the output voltage.

1.2 Summary of CAN data frames

DATA _DIR	DATA_ID Bit 7	6	5	4	3	2	1	0	Access	read/ write/ active	DATA - Bytes
	0	x	x	x	x	x	x	x	no DATA_ID		
	1	**0**	**C2**	**C1**	**C0**	**0**	**N1**	**N0**	Single access CHANNEL: N1=0, N0=1 ⇨ Channel A 1. N1=1, N0=0 ⇨ Channel B		
1	1	0	0	0	0	0	N1	N0	Actual voltage	r	5
1	1	0	0	1	0	0	N1	N0	Actual current	r	5
1/0	1	0	1	0	0	0	N1	N0	Set voltage	r/w	4
1/0	1	0	1	1	0	0	N1	N0	Ramp speed	r/w	2
0	1	0	0	0	1	0	N1	N0	Start voltage change	w	1
1	1	0	0	1	1	0	N1	N0	Hardware limits	r	4
1/0	1	0	1	0	1	0	N1	N0	Current trip	r/w	4
1/0	1	0	1	1	1	0	N1	N0	Auto start	r/w	2
1/0	1	0	1	1	0	1	N1	N0	Expanded ramp speed	r/w	3
	1	**1**	**C3**	**C2**	**C1**	**C0**	**G1**	**G0**	**Group access MODULE:** **G1 = G0 = 0, only needed if group controller (GC) is used**		
1/0	1	1	0	0	0	0	G1	G0	General status module / Advanced calibration	r/w	2
1	1	1	0	0	0	1	G1	G0	Module status Channel A and B	r	3
1	1	1	0	0	1	0	G1	G0	LAM-status Channel A and B	r	3
1	1	1	0	1	1	0	G1	G0	Log-on Front-end device in superior layer	a	3
0	1	1	0	1	1	0	G1	G0	Log-off superior layer at Front-end device	w	3
0	1	1	0	1	1	1	G1	G0	New bit rate	w	3
1	1	1	1	0	0	0	G1	G0	Serial number, software release and channels	r	7
							C_i		Commands		

	N_i	Channels A and B
	G_i	Group 0 to 3 Only needed if a group controller (GC) is used

1.3 Detailed CAN data frames description

Log-on and Log-off Front-end (FE) device (active/write access)

Log-on frame of the module (DLC = 3)

Byte		DATA_ID								DATA_1		DATA_0							
Bit		7	6	5	4	3	2	1	0		0	7	6	5	4	3	2	1	0
Designation	DATA _DIR							G1	G0										
Data	1	1	1	0	1	1	0	0	0		x	0	0	0	0	1	0	1	1
Description	active	G1 to G0: Group 0 to 3 Only necessary if a group controller (GC) is used								x=1: General module status ok x=0: current limit/trips or voltage limit have been exceeded in at least one channel		Module class							

After POWER ON the module will send this group access command cyclically on the bus (ca. 2...10 sec).

Bit 0 in DATA_1 contains the general module status (logical NOR of the error bits LAM_REG2ER_, LAM_REG1ER_, LAM_EXTINH_ and LAM_ILIM_ in both channels).

If a controller identifies this command the module can be registered there as a Front-end device and addressed with FE_ADR.

(Module address, see also item 6.5, description 11bit-Identifier and item 6.6)

Remote-frame Log-on by the controller (DLC = 3)

Byte		DATA_ID								DATA_1		DATA_0							
Bit		7	6	5	4	3	2	1	0		0	7	6	5	4	3	2	1	0
Designation	DATA _DIR							G1	G0										
Data	0	1	1	0	1	1	0	0	0		1	0	0	0	0	1	0	1	1
Description	write	G1 to G0: Group 0 to 3 Only necessary if group controller (GC) is used								Log-on module		Module class							

After a successful registration the module will not send further Log-on frames as long as it receives accesses from the external CAN Bus in periods shorter than one minute or until it receives a Log-off frame from the controller:

Remote-frame Log-off controller (DLC = 3)

Byte		DATA_ID								DATA_1		DATA_0							
Bit		7	6	5	4	3	2	1	0		0	7	6	5	4	3	2	1	0
Designation	DATA _DIR							G1	G0										
Data	0	1	1	0	1	1	0	0	0		0	0	0	0	0	1	0	1	1

Description		write		G1 to G0: Group 0 to 3 Only needed if group controller (GC) is used	Log-off module	Module class

Single CHANNEL access: Actual voltage (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0
assignment	1	1	0	0	0	0	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):

Read actual voltage from the corresponding channel

⇓ Response module (DLC = 5)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0
assignment	0	1	0	0	0	0	0	x	x
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Byte	DATA_3			DATA_2			DATA_1			DATA_0		
Bit	7	...	0		...	0	7	...	0	7	...	0
Designation									LSB			LSB
assignment	x									x		
Description	Actual voltage [V]: exponential representation mantissa in 24-bit binary notation in DATA_3, DATA_2 und Data_1, exponent with sign in DATA_0											

Single CHANNEL access: Actual current (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0
Data	1	1	0	0	1	0	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):

Read actual current from the corresponding channel

⇓ Response module (DLC = 5)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0
Data	0	1	0	0	1	0	0	x	x
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Byte	DATA_3			DATA_2			DATA_1			DATA_0		
Bit	7	...	0		...	0	7	...	0	7	...	0
Designation									LSB			LSB
Data	x									x		
Description	Actual current [A]: exponential representation mantissa in 24-bit binary notation in DATA_3, DATA_2 und Data_1, exponent with sign in DATA_0											

Single CHANNEL access: Set voltage (Read-write/Write access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0
Data	1	1	0	1	0	0	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):
Read set voltage from the corresponding channel

⇓ Response module (DLC = 4)

Byte		DATA_ID								DATA_2			DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0	7	...	0
Designation	DATA _DIR							N1	N0									LSB
Data	0	1	0	1	0	0	0	x	x	X								
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								Set voltage in [0,1V] in DATA_2, DATA_1 and DATA_0								

Write [Controller (DLC = 4): Write set voltage to corresponding channel]

Byte		DATA_ID								DATA_2			DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0	7	...	0
Designation	DATA _DIR							N1	N0									LSB
Data	0	1	0	1	0	0	0	x	x	X								
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								Set voltage in [0,1V] in DATA_2, DATA_1 and DATA_0								

Set voltages which are higher than the maximum voltage of the channel (nominal module voltage or V_{max}) will be limited to the maximum voltage.

Single CHANNEL access: Ramp speed (Read-write/Write access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0
Data	1	1	0	1	1	0	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):

Read actual ramp speed from the corresponding channel

⇓ Response module (DLC = 2)

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0								LSB
Data	0	1	0	1	1	0	0	x	x	x7	x6	x5	x4	x3	x2	x1	x0
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								x7 … x0: Ramp speed (1 to 255 V/s)							

Write [Controller (DLC = 2): Write ramp speed to the corresponding channel]

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0								LSB
Data	0	1	0	1	1	0	0	x	x	x7	x6	x5	x4	x3	x2	x1	x0
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								x7 … x0: Ramp speed (1 to 255 V/s)							

Ramp speed lower than 1 V/s will be set to 1 V/s by the firmware.
This is also the default value when powering up the module, except a different value has been saved using the function „Auto start“.

If the voltage ramp is changed while the voltage is ramping, the changes are taken over immediately, i.e. the channel will resume to ramp with the new ramp speed value.

Special note when using Single CHANNEL access: Expanded ramp speed (see page 13)

If the command "Expanded ramp speed" is used to write a ramp speed where

1st the value is not integer and

2nd the value is not in the range from 1 V/s to 255 V/s,

the module will respond with value 0 in DATA_0.

Single CHANNEL access: Expanded ramp speed (Read-write/Write access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0
Data	1	1	0	1	1	0	1	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):

Read actual ramp speed from the corresponding channel

in expanded resolution

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0																LSB
Data	0	1	0	1	1	0	1	x	x	x15							x8	x7							x0
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								x15 … x0: Ramp speed with resolution 0,1 V/s (up 0,1 V/s to 2500 V/s)															

Write [Controller (DLC = 3): Write expanded ramp speed to the corresponding channel]

Byte		DATA_ID								DATA_1								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0																LSB
Data	0	1	0	1	1	0	1	x	x	x15							x8	x7							x0
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								x15 … x0: Ramp speed with resolution 0,1 V/s (up 0,1 V/s to 2500 V/s)															

Ramp speed lower than 0,1 V/s will be set on 0,1 V/s by the firmware.

The default value when powering up the module is 1,0 V/s, except a different value has been saved using the function „Auto start".

If the voltage ramp is changed while the voltage is ramping, the changes are taken over immediately, i.e. the channel will resume to ramp with the new ramp speed value.

Please note the connection with **Single CHANNEL access: Ramp speed** (see page 12)!

Single CHANNEL access: Start (Write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0
Data	0	1	0	0	0	1	0	x	x
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):

Start voltage change in the corresponding CHANNEL.

If the output voltage has been switched off permanently by exceeding V_{max} , I_{max} or in the presence of an INHIBIT signal with ENABLE KILL or programmable current trips,
it is necessary to READ the LAM-Status in the register LAM_REG1ER, LAM_EXTINH or LAM_ILIM to reset it, before the output voltage can be restored.

If the output voltage has been limited by V_{max} or I_{max} in case of DISABLE KILL (ERROR-LED flashes and LAM_REG2ER_= 1), the output voltage can be decreased by writing of a lower set voltage and a following „Start“ (Error-LED stops flashing). A subsequent increase of the voltage, however, is only possible after resetting the register LAM_REG2ER_ by a READ of register LAM-status.

Single access CHANNEL: Limit (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR							N1	N0
Data	1	1	0	0	1	1	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):

check Hardware limit settings in the corresponding CHANNEL

⇓ Response module (DLC = 4)

Byte		DATA_ID								DATA_2			DATA_1						DATA_0					
Bit		7	6	5	4	3	2	1	0	7	...	0	7	..	4	3	..	0	7	..	4	3	..	0
Designation	DATA_DIR							N1	N0			LSB		..			..			..	LSB		..	
Data	0	1	0	0	1	1	0	x	x	x			x			x						x		
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								mantissa V_{max} (8 bit)			Exp.V_{max}			mantissa I_{max} (8 bit)						exp I_{max}		

exp. (4 bit), for exp. > 7 results in: negative exponent in 2´er complement

Single CHANNEL access: Current trip (Read-write//Write access)

Read-write access

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0
Data	1	1	0	1	0	1	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):
Read maximum output current (current trip)
from the corresponding CHANNEL .

⇓ Response module (DLC = 4)

Byte		DATA_ID								DATA_2			DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0	7	...	0
Designation	DATA _DIR							N1	N0									LSB
Data	0	1	0	1	0	1	0	x	x	x								
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								Current trip [A]: exponential representation mantissa in 24-bit binary notation in DATA_3, DATA_2 und Data_1, without exponent. Exponent is the same as the value for the upper current measurement range.								

Write access [Controller (DLC = 4): set max. output current (current trip) in corresponding CHANNEL]

Byte		DATA_ID								DATA_2			DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0	7	...	0
Designation	DATA _DIR							N1	N0									LSB
Data	0	1	0	1	0	1	0	x	x	x								
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								Current trip [A]: exponential representation mantissa in 24-bit binary notation in DATA_3, DATA_2 und Data_1, without exponent. Exponent is the same as the value for the upper current measurement range.								

If the output current exceeds the programmed current limit then the output voltage will be switched off by the software (current trip). The resolution for the current limit is the same as the resolution of the current measurement. For the current limit = 0 A current trip is deactivated.
If the output voltage has been switched off by the exceeding of the maximum current, the LAM–status must be read in order to resume the output voltage generation with „Start“ or active „Auto start“ again.

Single CHANNEL access: Auto start (Read-write//Write access)

Read-write access

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0
Data	1	1	0	1	1	1	0	x	x
Description	read	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B							

Controller (DLC = 1):
Check if „Auto start“ of corresponding CHANNEL is active.

⇓ Response module (DLC = 2)

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0								LSB
Data	0	1	0	1	1	1	0	x	x					x3			
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								x3 = 1: Auto start is active x3 = 0: Auto start not active							

Auto start active means:

- if the 'Auto start' conditions (module-status ON_OFF_+ IN_EX_= 0 and LAM-Status _REG2ER_+_REG1ER_+_EXTINH_+_ILIM_= 0) are satisfied, the output voltage of the CHANNEL will be ramped to the active set voltage, i.e. „Start“ is not required after 'Write set voltage' **,** Power-ON and Power OFF⇒ ON.
- if the output voltage of the CHANNEL has been switched off permanently by the exceeding V_{max}, I_{max} or in the presence of an INHIBIT (in case of ENABLE KILL or Current Trip), it will be restored with software ramp after reading the LAM-status.
- if the output voltage is limited by V_{max} or I_{max} in case of DISABLE KILL (ERROR-LED flashing and LAM_REG2ER_= 1), the output voltage can be decreased by writing a lower set voltage (Error-LED stops flashing). A subsequent increase of the voltage, however, is only possible after resetting the register LAM_REG2ER_ by a READ of register LAM-status.

Write access [Controller (DLC = 2): activate Auto start for corresponding CHANNEL]

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA _DIR							N1	N0								LSB
Data	0	1	0	1	1	1	0	x	x					x3	x2	x1	x0
Description	write	N1=0, N0=1 ⇨ Channel A N1=1, N0=0 ⇨ Channel B								x3 = 1: Auto start activate							

x2 = 1: actual current trip ⎫ store
x1 = 1: actual set voltage ⎬ in EEPROM
x0 = 1: actual voltage ramp ⎭ one time

Values will be restored in corresponding register after connecting the supply voltages!
(for EEPROM 1 Million writing cycles guaranteed)

Group access: General module status (Read-write access)

Read-write access

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA _DIR								
Data	1	1	1	0	0	0	0	0	0
Description	read								

Controller (DLC = 1):
Read general module status

⇓ Response module (DLC = 2)

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA _DIR																LSB
Data	0	1	1	0	0	0	0	0	0	1	1	1	b4	1	1	b1	b0
Description	write									b4: fine adjustment b1: ramp status b0: sum status							

Write access [Controller (DLC = 2): Switch fine adjustment off or on]

Byte		DATA_ID								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA _DIR																LSB
Data	0	1	1	0	0	0	0	0	0	X	X	X	b4	X	X	X	X
Description	write									B4: fine adjustment X: any							

Bit	Name	Description	0	1
b4	ADVANCED STATUS	1. Fine adjustment	off	on
b1	RAMP STATUS	Voltage is ramping	yes	no
b0	SUM STATUS	No error bit active	no	yes

The purpose of the fine adjustment is to compensate long time and temperature drifts of the DAC. If the fine adjustment is active, the output voltage is compensated such that the average of the measured voltage is equal to the set voltage.
The corresponding status bit (bit 4) is set by default, i.e. the fine adjustment is on. It can be switched off by writing the general module status with bit 4 = 0.

The RAMP STATUS (bit 1) is set, if V_{OUT} is stable in both channels (no changing with ramp).

The SUM STATUS (bit 0) is generated by a combination of the error bits LAM_REG2ER_, LAM_REG1ER_, LAM_EXTINH_ and

LAM_ILIM_ in both channels with a logical NOR. The SUM STATUS is set if none of these errors have occured.

Group access: module status CHANNEL A and B (Read-write access)

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA _DIR								
Data	1	1	1	0	0	0	1	0	0
Description	read								

Controller (DLC = 1):

READ module - status of channels

⇓ Response module (DLC = 3)

Byte		DATA_ID								DATA_1			DATA_0		
Bit		7	6	5	4	3	2	1	0	7	...	0	7	...	0
Designation	DATA _DIR									CHANNEL B			CHANNEL A		
Data	0	1	1	0	0	0	1	0	0	x					
Description	write									see list					

Description				Module-status CHANNEL A and B (read)		
CHANNEL	DATA	Bit	Name	Description	0	1
B	**_1**	b7	ERROR_2	error in CHANNEL B	channel ok	error
		b6	STATV_2	status V_{out}	V_{out} stable	V_{out} in change
		b5	TRENDV_2	Moving direction of V_{out}	V_{out} falling	V_{out} rising
		b4	KILL_2	*switch position KILL*	disabled	enabled
		b3	ON_OFF_2	*Switch position HV-ON/OFF*	on	off
		b2	POL_2	Polarity of output voltage V_{out}	negative	positive
		b1	IN_EX_2	*Switch position CONTROL*	DAC	manual
		b0	VZ_2	*Output voltage V_{out} CHANNEL B*	V_{out}<>0	V_{out}=0
A	**_0**	b7	ERROR_1	Error in CHANNEL A	channel ok	error
		b6	STATV_1	status V_{out}	V_{out} stable	V_{out} in change
		b5	TRENDV_1	Moving direction of V_{out}	V_{out} falling	V_{out} rising
		b4	KILL_1	*switch position KILL*	disabled	enabled
		b3	ON_OFF_1	*Switch position HV-ON/OFF*	on	off
		b2	POL_1	Polarity of output voltage V_{out}	negative	positive
		b1	IN_EX_1	*Switch position CONTROL*	DAC	manual
		b0	VZ_1	*Output voltage V_{out} CHANNEL B*	V_{out}<>0	V_{out}=0

Group access: LAM-status CHANNEL A and B (Read-write access)

Byte / Bit		DATA_ID 7	6	5	4	3	2	1	0
Designation	DATA _DIR								
Data	1	1	1	0	0	1	0	0	0
Description	read								

Controller (DLC = 1):
READ module - Status of channels

⇓ Response module (DLC = 3)

Byte / Bit		DATA_ID 7	6	5	4	3	2	1	0	DATA_1 7 … 0	DATA_0 7 … 0
Designation	DATA _DIR									CHANNEL B	CHANNEL A
Data	0	1	1	0	0	1	0	0	0	x	
Description	write									See list	

Description				LAM-Status CHANNEL A and B (read)	
CHANNEL	DATA	Bit	Name	Description for Bit = 1	remarks
B	_1	b7	LAM_REG2ER_2	*Quality of output voltage in CHANNEL B is not guaranteed at time*	
		b6	LAM_REG1ER_2	*V_{max} or I_{max} was/is exceeded*	
		b5	LAM_EXTINH_2	*external Inhibit-signal was / is active*	
		b4	LAM_RANGE_2	relation V_{nom} to V_{max} > 1	Set voltage > V_{max}
		b3	LAM_KEY_CHANGED	A front panel switch of CHANNEL B has been activated	ON_OFF_2, IN_EXT_2, KILL_2
		b2	LAM_EOP_2	V_{out} CHANNEL B arrived at set voltage	end of process_2
		b1	LAM_ILIM_2	I_{out} has been higher than programmed I_{max} (current trip CHANNEL B)	
		b0			
A	_0	b7	LAM_REG2ER_1	*Quality of output voltage in CHANNEL A is not guaranteed at this moment.*	
		b6	LAM_REG1ER_1	*V_{max} or I_{max} was/is exceeded*	
		b5	LAM_EXTINH_1	*external Inhibit-signal was/ is active*	
		b4	LAM_RANGE_1	Relation V_{nom} to V_{max} > 1	Set voltage > V_{max}
		b3	LAM_KEY_CHANGED	A front panel switch of CHANNEL A has been activated	ON_OFF_1, IN_EXT_1, KILL_1
		b2	LAM_EOP_1	V_{out} CHANNEL A arrived at set voltage	end of process_1
		b1	LAM_ILIM_1	I_{out} has been higher than programmed I_{max} (current trip CHANNEL A)	
		b0			

Status bits will be set if a corresponding event happens and reset if LAM-status has been read afterwards. If the event is still existing or if it happens again the corresponding bits will be set again.

Group access: New bit rate (Write access)

Controller (DLC = 3): „ write new bit rate“ into EEPROM.

Byte		DATA_ID								DATA_1								DATA_0							
Bit		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Designation	DATA _DIR																								LSB
Data	0	1	1	0	1	1	1	0	0								x8	x7	x6	x5	X4	x3	x2	x1	x0
Description	write									-7 bit rates are possible 1) 20 kBit/s 2) 50 kBit/s 3) 100 kBit/s 4) 125 kBit/s 5) 250 kBit/s 6) 500 kBit/s only on request 7) 1000 kBit/s only on request -the new bit rate becomes active only after RESET or POWER OFF/ON and -it has to be ensured, that all modules of one segment have been set to the same bit rate before a RESET or POWER OFF/ON, -the default (factory set) bit rate can be found on a label on the connector.															

Group access: Serial number and Software release (Read-write access)

Read-write

Byte		DATA_ID							
Bit		7	6	5	4	3	2	1	0
Designation	DATA_DIR								
Data	1	1	1	1	0	0	0	0	0
Description	read								

Controller (DLC = 1):

Read serial number, software release and the number of channels

⇓ Response module (DLC = 7)

Byte		DATA_ID								DATA_5		DATA_4		DATA_3		DATA_2		DATA_1		DATA_0	
Bit		7	6	5	4	3	2	1	0	BCD	BCD	BCD	BCD	BCD	BCD	BCD	BCD	BCD	BCD	BCD	BCD
Designation	DATA_DIR																				
Data	0	1	1	1	0	0	0	0	0	z6	z5	z4	z3	z2	z1	0	y3	y2	y1	0	x1

Description		write			z_n : 6 BCD Serial number	y_n : 3 BCD software release	x1: 1 BCD existing channels

1.4 Implementation in CAN-Bus

The data frame structure is matched to the message frame of the standard-format according to CAN specification 2.0B. The data transfer is realized using an in-house Device Control Protocol (DCP.)

The data frame of the DCP is transferred as data-word with n bytes length in the data field of the CAN frames according to the specific demands of the respective access. This results in a Data Length Code (DLC) of the CAN-protocol of n.

A Front-end device is addressed using the 11 bit identifier of the CAN protocol (for setting of the module address see also section 6.6). It is possible to address up 64 NHQ devices with a CAN interface on a single bus (64 nodes).

ID10 and ID9 are 0,

ID8 to ID3 allows the addressing of 64 iseg Front-end devices (ID3: A0 = 2^0 ;...; ID8: A5 = 2^5),

ID1 and ID2 are not used.

ID0 is the data direction bit (DATA_DIR)

The RTR Bit is always set to zero.

All modules on a single CAN-Bus segment must have a unique identifier and must use the same bit rate. The factory fixed bit rate can be found on the label on the connector.

The information on the data transfer direction (DATA_DIR) is given by the low-end bit ID0 of the 11 Bit CAN-Identifier. The controller requests read data with DATA_DIR=1 and sends data to be written with DATA_DIR = 0. The Front-end device responds to read data request by sending the corresponding data with DATA_DIR = 0.

Only in the case the Front-end device is not registered to the controller or it does not receive any valid data during a longer time period (about 1 min), it will actively send the registration frame with DATA_DIR = 1 (see also section 6.4).

In the summary this means that all even CAN-ports (Identifier) are interpreted as 'Write ports' all odd CAN ports as ' Read ports'.

Thus structure for the control of a Front-end device in this lowest CAN segment is given by:

S	Identifier	R			DLC	n – data bytes				CRC	Ack
O		T	0	0	(n = 1 - 8)	DATA_ID	DATA_(n-2) ≥ 0	DATA_(n-3) ≥ 0	DATA_ ...		F.
F	b11 b0	R	reserv		b3 b0	**b7=** b0	b7 b0	b7 b0	b7 b0	15 bit	

ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	0	A5	A4	A3	A2	A1	A0			DATA _DIR
Acceptance-Filter of the used CAN-Controller is set to Front-end-address										

The Front-end device must perform the following tasks:

- Processing of single channel commands
- Processing of group information for the channels
- Active registration to the controller by sending the module address
- Generation of status information.

The electrical transmission is galvanically isolated and works with signal CAN_L and CAN_H, relative to CAN_GND. The pin assignment of the D-Sub-9 connector is shown in this list. Storing the module address (identifier) in EEPROM

PIN	Signal	description
2	CAN_L	
3	CAN_GND	GND
5	CAN_SHLD	shield
7	CAN_H	

1. Before the module is powered up by switching on the supply voltages (± 24V; ± 6V) the following switch configuration must be set for both channels
   ⇨ switch CONTROL [10] on MANUAL; ⇨ switch HV-ON [9] on OFF;
   ⇨ switch KILL [12] on ENABLE.
2. Switch ON the supply voltages.
3. After the Power-On-Test the LCD-display [1] shows an 'A' on left hand side and on right hand side the current address in HEX, e.g. 00 with a flashing hyphen in between.
4. By switching the measuring switch [3] and the channel switch [2] the address can be modified between 00 and 3F.
5. The address can be stored to the EEPROM using the switch KILL [12], the module is ready to operate.
6. If there is no change within 10s and no switching of the CONTROL, KILL or HV-ON switches the new address is discarded, the module will keep the previous address.

1.5 Resetting the module

The module will be reset to the factory settings with the following procedure:

1. Set the module address to a value different from 00 (see point 6.6)
2. Set the module address to 00.

The module is set to the factory settings.

2. Software

Contact us for an overview on our user friendly control and data acquisition software.

3. Manufacturers contact

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