Precision VME High Voltage Power Supply

Option(s) VME Interface

Attention!

-It is not allowed to use the unit if the covers have been removed.

-We decline all responsibility for damages and injuries caused by an improper use of the module. It is highly recommended to read the operators manual before any kind of operation.

Note

The information in this manual is subject to change without notice. We take no responsibility whatsoever for any error in the document. We reserve the right to make changes in the product design without reservation and without notification to the users.

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1.3 Interlock Output

The Interlock Output is a static TTL signal which is active at Low level on the safety loop connector on the front panel. The function Interlock input (see position 1. General Information) is not available in this option.
The Interlock Output signal can be generated when the control signal SetKilEenable of the ModuleControl register (see 2.2.1 Module Registers) is not set. This status is to be observed by the bit IsKilEnable of the ModuleStatus register.

Interlock Output is active in 2 cases:

A: After Power On reset
After Power On reset the Interlock Output system waits for handling all channels. The Interlock Output is active. This state is indicated by ModuleInterlockOutStatus.IsILKStandBy ==1.

This state is ended by one of the following actions:

1. Each channel must be switched on one times in minimum. The channels should be initialized by setting the demand voltage Vset and switching the channel on. If one channel isn't used in the system, it must be switched on also. After that it can be switched off.
2. The Interlock Output system is reset. Therefore the bit ModuleInterlockOutControl.SetILKEnable must be cleared and after that set.

B: When any of the following conditions in any channel of the module is true:

1. VoltageMeasure is equal or greater than the actual maximal Voltage (VoltageLimit) of the channel. This is shown by active bit "isVLIM" of the ChannelStatus register. The VoltageLimit is calculated by channel's VoltageNominal multiplied by VoltageMax of the front panel potentiometer.
2. VoltageMeasure exceeds the VoltageBounds
This is shown by active bit "isVBNDS" of the ChannelStatus register
3. CurrentMeasure is equal or greater than the actual maximal Current (CurrentLimit) of the channel. This is shown by active bit "isCLIM" of the ChannelStatus register. The CurrentLimit is calculated by channel's CurrentNominal multiplied by CurrentMax of the front panel potentiometer.
4. CurrentMeasure exceeds the CurrentBounds
This is shown by active bit "isCBNDS" of the ChannelStatus register
5. CurrentMeasure is equal or greater than CurrentSet
The channel will switch to current control; this is shown by active bit "isCC" in ChannelStatus register

For monitoring and control of the Interlock Output function, some auxiliary bits and registers are defined in the module.

1.4 Interlock Event Output

The Interlock Event Output is a static TTL signal which is active at Low level on the safety loop connector on the front panel. The function Interlock input (see position 1. General Information) is not available in this option. The Interlock Event Output signal can be generated when the control signal SetKilEenable of the ModuleControl register (see 2.2.1 Module Registers) is set or not set. This status is to be observed by the bit IsKilEnable of the ModuleStatus register.

Interlock Output is active in 2 cases:

A: After Power On reset
After Power On reset the Interlock Output system waits for handling all channels. The Interlock Output is active. This state is indicated by ModuleInterlockOutStatus.IsILKStandBy ==1.

This state is ended by one of the following actions:

1. Each channel must be switched on one times in minimum. The channels should be initialized by setting the demand voltage Vset and switching the channel on. If one channel isn't used in the system, it must be switched on also. After that it can be switched off.
2. The Interlock Output system is reset. Therefore the bit ModuleInterlockOutControl.SetILKEnable must be cleared and after that set.

B: When any of the following conditions in any channel of the module is true:

1. VoltageMeasure is equal or greater than the actual maximal Voltage (VoltageLimit) of the channel. This is shown by active bit "EVLIM" of the ChannelEventStatus register. The VoltageLimit is calculated by channel's VoltageNominal multiplied by VoltageMax of the front panel potentiometer.
2. VoltageMeasure exceeds the VoltageBounds
This is shown by active bit "EVBNDS" of the ChannelEventStatus register
3. CurrentMeasure is equal or greater than the actual maximal Current (CurrentLimit) of the channel. This is shown by active bit "ECLIM" of the ChannelEventStatus register. The CurrentLimit is calculated by channel's CurrentNominal multiplied by CurrentMax of the front panel potentiometer.
4. CurrentMeasure exceeds the CurrentBounds
This is shown by active bit "ECBNDS" of the ChannelEventStatus register
5. CurrentMeasure is equal or greater than CurrentSet - ModuleControl register setKILE=0
The channel will switch to current control; this is shown by active bit "ECC" in ChannelEventStatus register
OR
CurrentMeasure has been exceeded the CurrentSet - ModuleControl register setKILE=1
The channel has caught an event trip; this is shown by active bit "ETRP" in ChannelEventStatus register

For monitoring and control of the Interlock Output function, some auxiliary bits and registers are defined in the module.

1.4.1 Overview of the Interlock Output Registers

Special Registers

Offset Bytes (rel. to BA)	Name	Data type	Access
0x0040	ModuleInterlockOutStatus	uint16	r
0x0042	ModuleInterlockOutControl	uint16	r/w
0x0044	ModuleInterlockCount	uint16	r
0x0046	ModuleInterlockLastTrigger	uint16	r
0x0048	ModuleInterlockChnActualActive	uint16	r
0x004a	ModuleInterlockChnEverTriggered	uint16	r

1.4.2 ModuleInterlockOutStatus

ModuleInterlockOutStatus

Offset Bytes (rel. to BA)	Name	Data type	Access
0x0040	ModuleInterlockOutStatus	uint16	r

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
isILKena	isILKact	res	res	res	res	res	res	res	res	res	res	isILKTL3	isILKTL2	isILKTL1	isILKTL0

isILKena	IsIlkEnabled	Interlock Output enabled (1) or disabled (0)
isILKact	IsIlkActive	Interlock Output signal active (any condition is true)
isILKstby	IsILKStandBy	Interlock Output signal active because of PowerOn reset and channels are not handled yet
isILKTL0..3	IsIlkTestLoops[0;1;2;3]	Counter for Stretching of the Interlock Test Pulse
Res	reserverd	reserved

1.4.3 ModuleInterlockOutControl

ModuleInterlockOutControl

Offset Bytes (rel. to BA)	Name	Data type	Access
0x0042	ModuleInterlockOutCommand	uint16	r/w

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
setILKena	clrILKregs	res	res	res	res	res	setILKCb	setILKVl	setILKVb	setILKCl	setILKIs	doILKTL3	doILKTL2	doILKTL1	doILKTL0

setILKena	SetIlkEnable	enable (1) or disable (0) Interlock Output
clrILKregs	ClearIlkRegisters	clear Interlock Out part registers
setILKCb	SetIlkCBnds	simulate Interlock Out triggered by Current Bounds
setILKVl	SetIlkVlim	simulate Interlock Out triggered by Vlimit
setILKVb	SetIlkVBnds	simulate Interlock Out triggered by Voltage Bounds
setILKCl	SetIlkClim	simulate Interlock Out triggered by Climit
setILKIs	SetIlkIset	simulate Interlock Out triggered by Iset
doILKTL	DoIlkTestLoops[0;1;2;3]	simulate an Interlock Out pulse of n * 40ms length; n= 1..15; n=0 => no test pulse
Res	reserverd	reserved

The register ModuleInterlockOutControl controls all work with the Interlock output part. The bit setIlkEnable enables or disables the output.
The output signal is generated when at least one of the interlock conditions (see chapter 1.3) is true. For test purposes, the generation of a test pulse can be initiated. To have a possibility to check the handler of the external control software, the generation of different trigger sources and pulse lengths is possible.

1.4.4 ModuleInterlockCount

ModuleInterlockCount

Offset Bytes (rel. to BA)	Name	Data type	Access
0x0044	ModuleInterlockCount	uint16	r

Counter of 16 bit unsigned integer to count different states of Interlock condition is true.
A true Interlock condition of a channel is counted only in case no other Interlock condition is active on the same channel (means, the corresponding channel bit in register ModuleInterlockChnActualActive is not set).

1.4.5 ModuleInterlockLastTrigger

ModuleInterlockLastTrigger

Offset Bytes (rel. to BA)	Name	Data type	Access
0x0046	ModuleInterlockLastTrigger	uint16	r/w

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
res	res	res	res	Chn3	Chn2	Chn1	Chn0	isILKVl	isILKVb	isILKCl	isILKIs	isILKCb	res	res	isIlkTst

Chn0..3	IlkChn [0;1;2;3]	number of the channel that initiated last trigger ; for testing: IlkChn = 15
isILKVl	IsIlkVlim	Interlock Out triggered by Vlimit
isILKVb	IsIlkVBnds	Interlock Out triggered by Voltage Bounds
isILKCl	IsIlkClim	Interlock Out triggered by Climit
isILKIs	IsIlkIset	Interlock Out triggered by Iset
IsILKCb	IsILKCBnds	Interlock Out triggered by Current Bounds
isILKTst	IsIlkTest	Last Interlock signal was simulated
res	reserverd	reserved

The register ModuleInterlockLastTrigger catches the information of the channel that triggered at last.
Such information are the channel number and the trigger source.
If an Interlock condition on this channel becomes active after the channel was registered as the last triggered channel, this new condition is added to the stored ones.
A new interlock condition at another channel (the corresponding channel bit in register ModuleInterlockChnActualActive was not active) overwrites the whole register.

1.4.6 ModuleInterlockChnActualActive

ModuleInterlockChnActualActive

Offset Bytes (rel. to BA)	Name	Data type	Access
0x0048	ModuleInterlockChnActualActive	uint16	r/w

ChannelList

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
res	Res	res	res	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

If a channel has an active Interlock condition at the moment, the corresponding channel bit is set. If the condition is resolved the corresponding bit is cleared.

1.4.7 ModuleInterlockChnEverTriggered

ModuleInterlockChnEverTriggered

Offset Bytes (rel. to BA)	Name	Data type	Access
0x004A	ModuleInterlockChnEverTriggered	uint16	r/w

ChannelList

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
res	Res	res	res	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

If a channel has an active Interlock condition, the corresponding channel bit is set. If the condition is resolved the corresponding bit remains set.